

FIG. 1

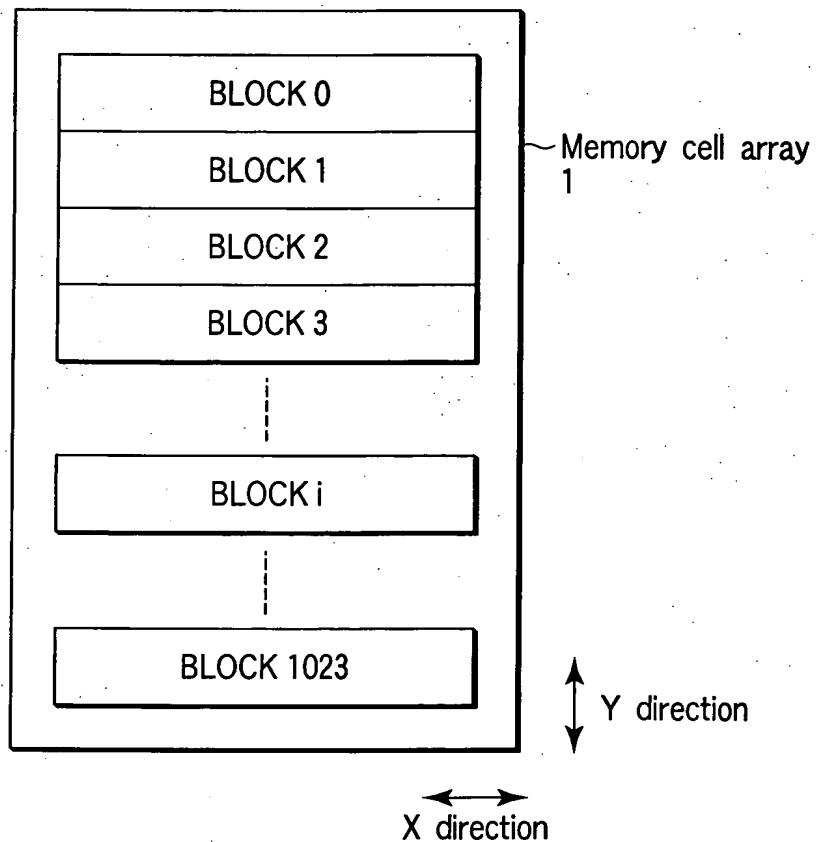


FIG. 2

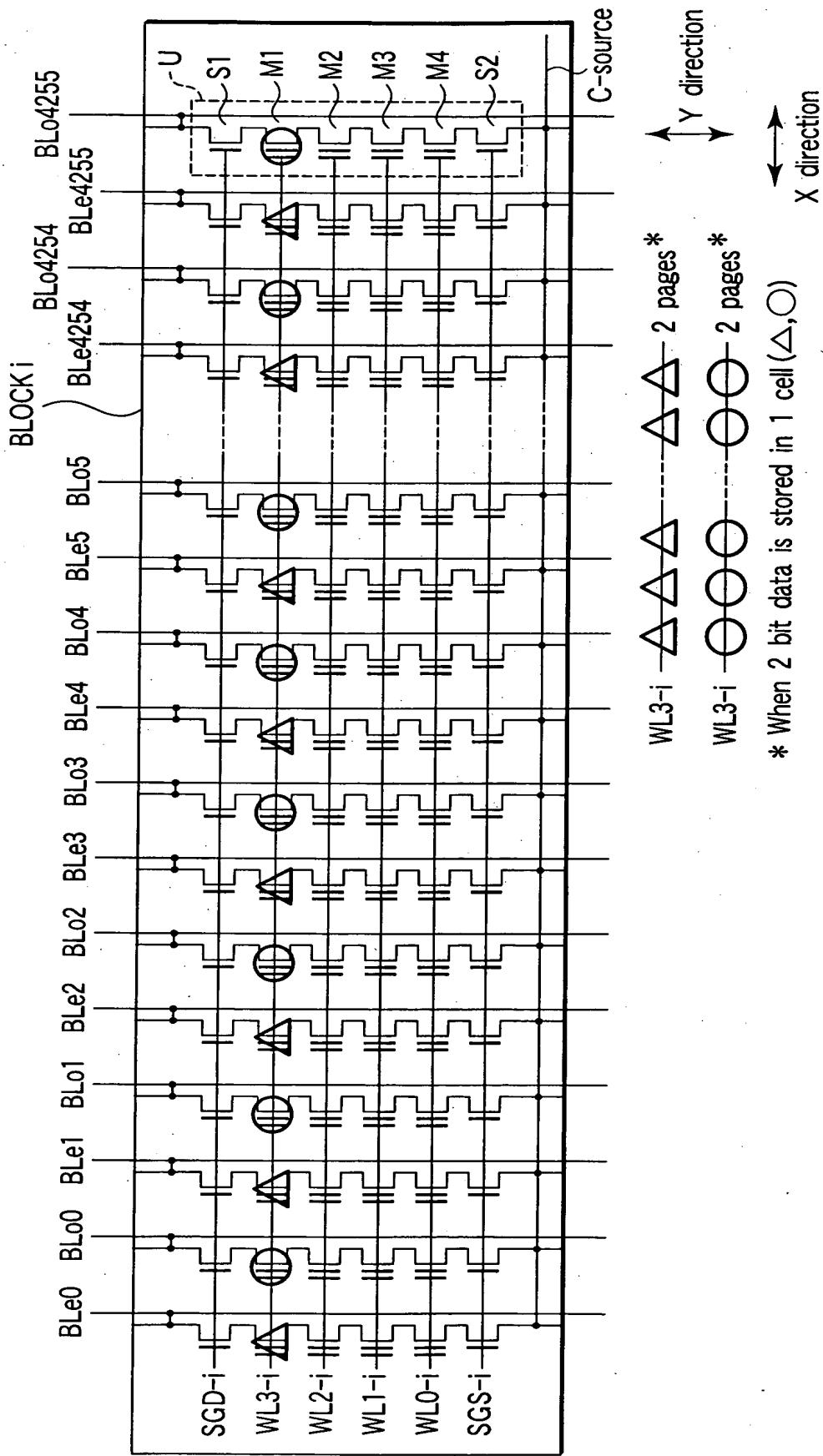


FIG. 3

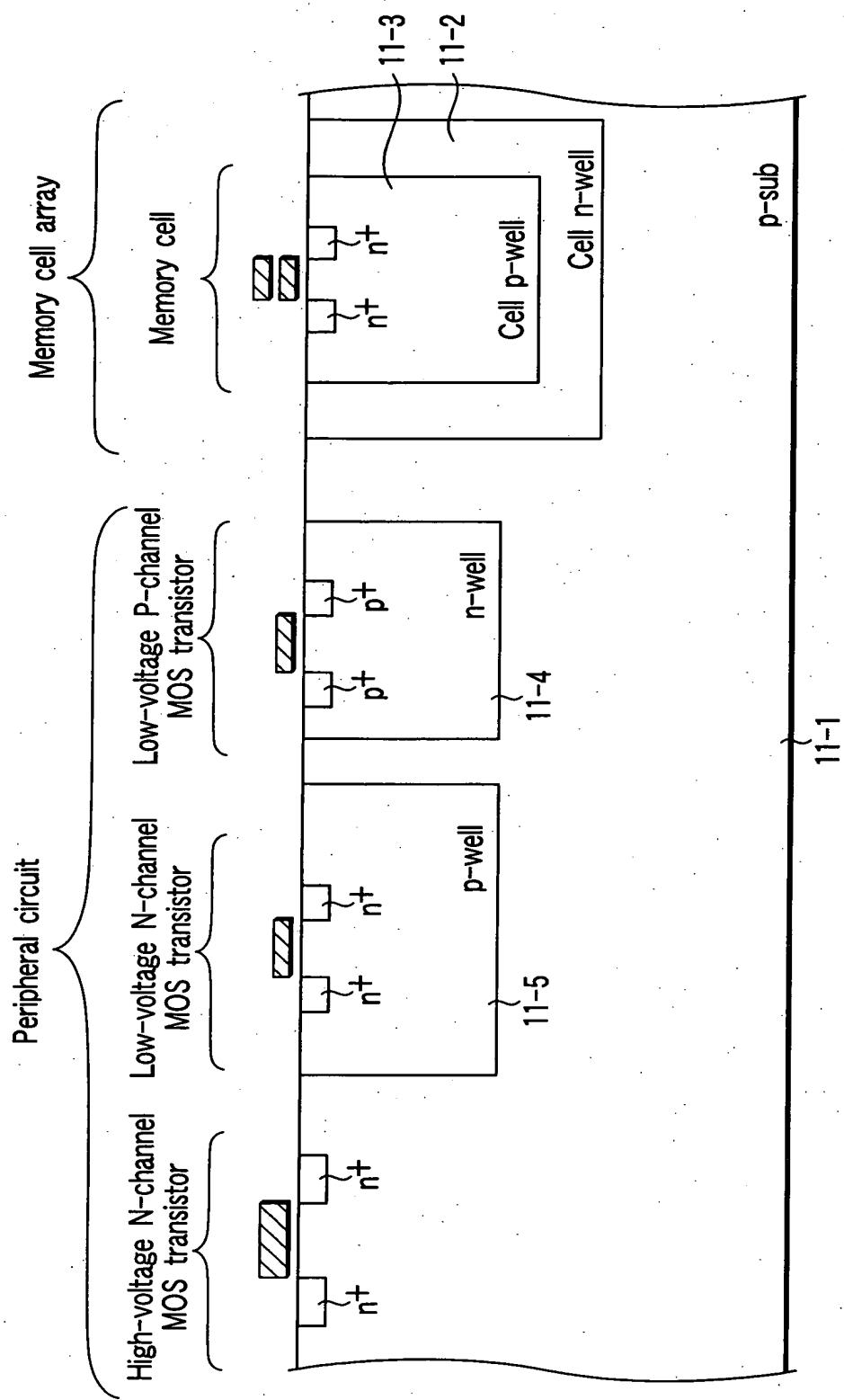
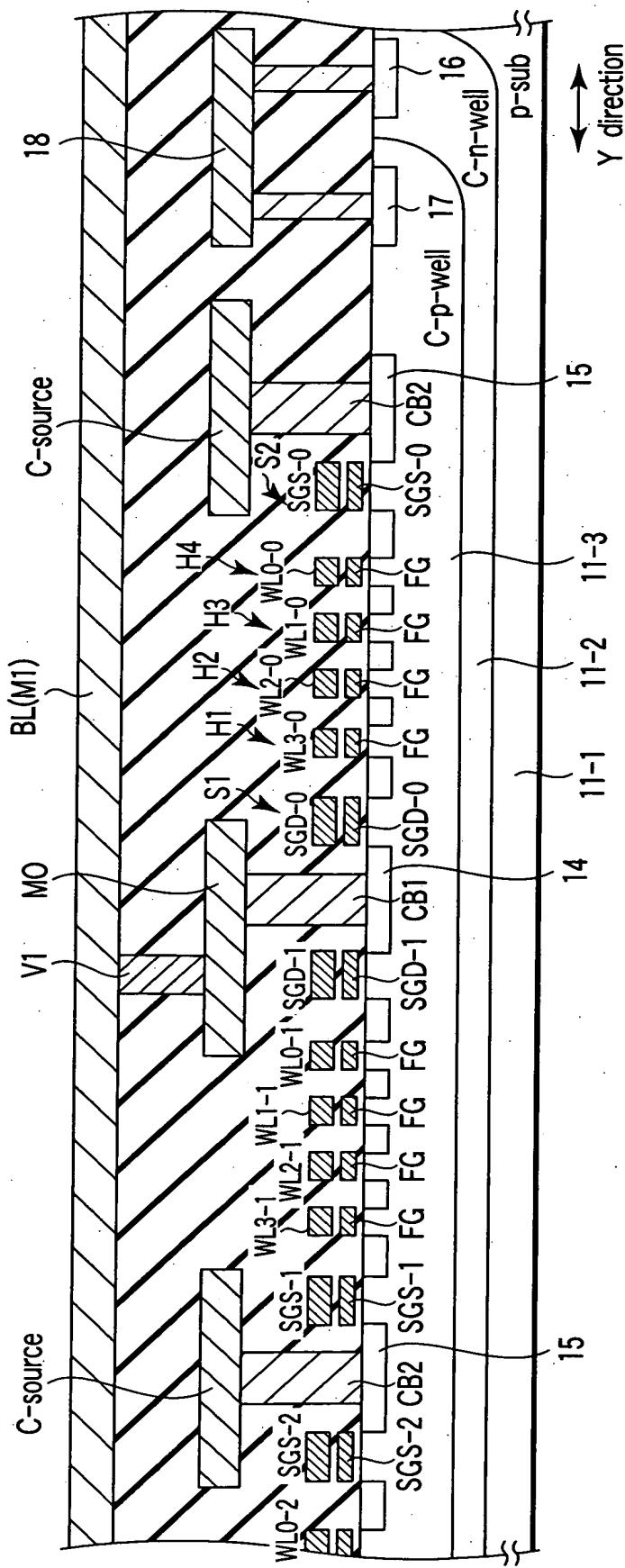


FIG. 4



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Memory cell

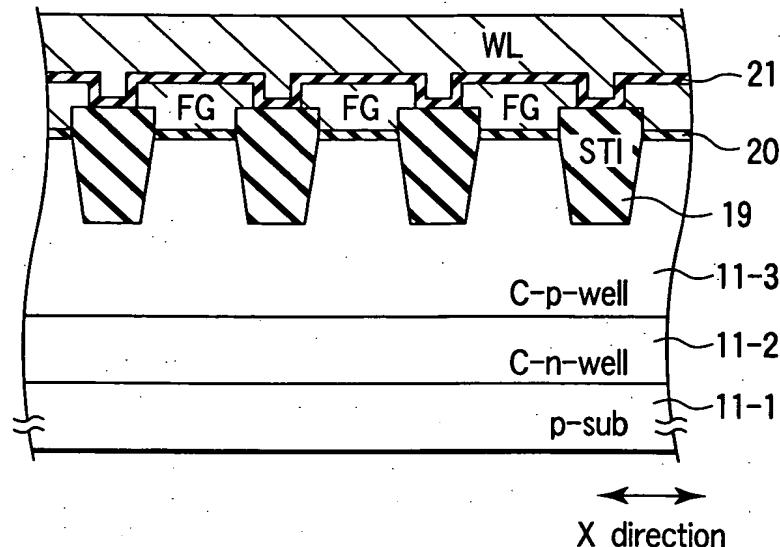


FIG. 6

Select gate transistor

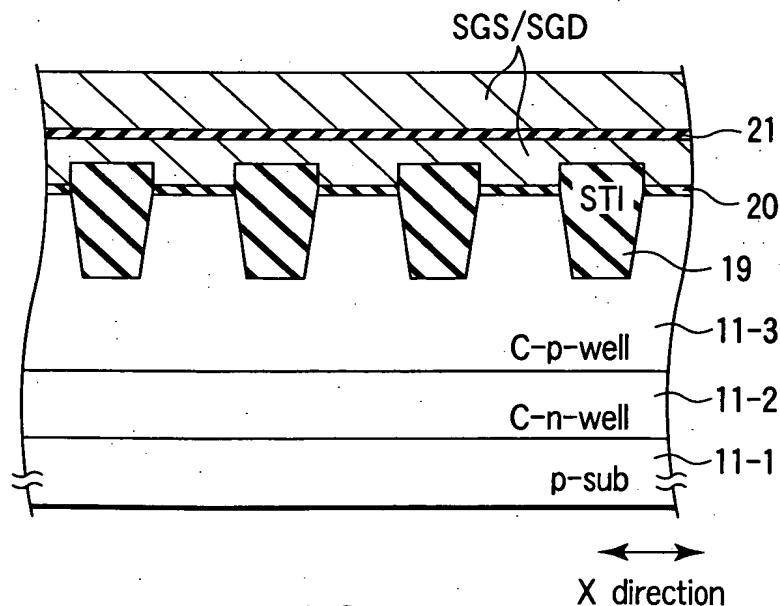


FIG. 7

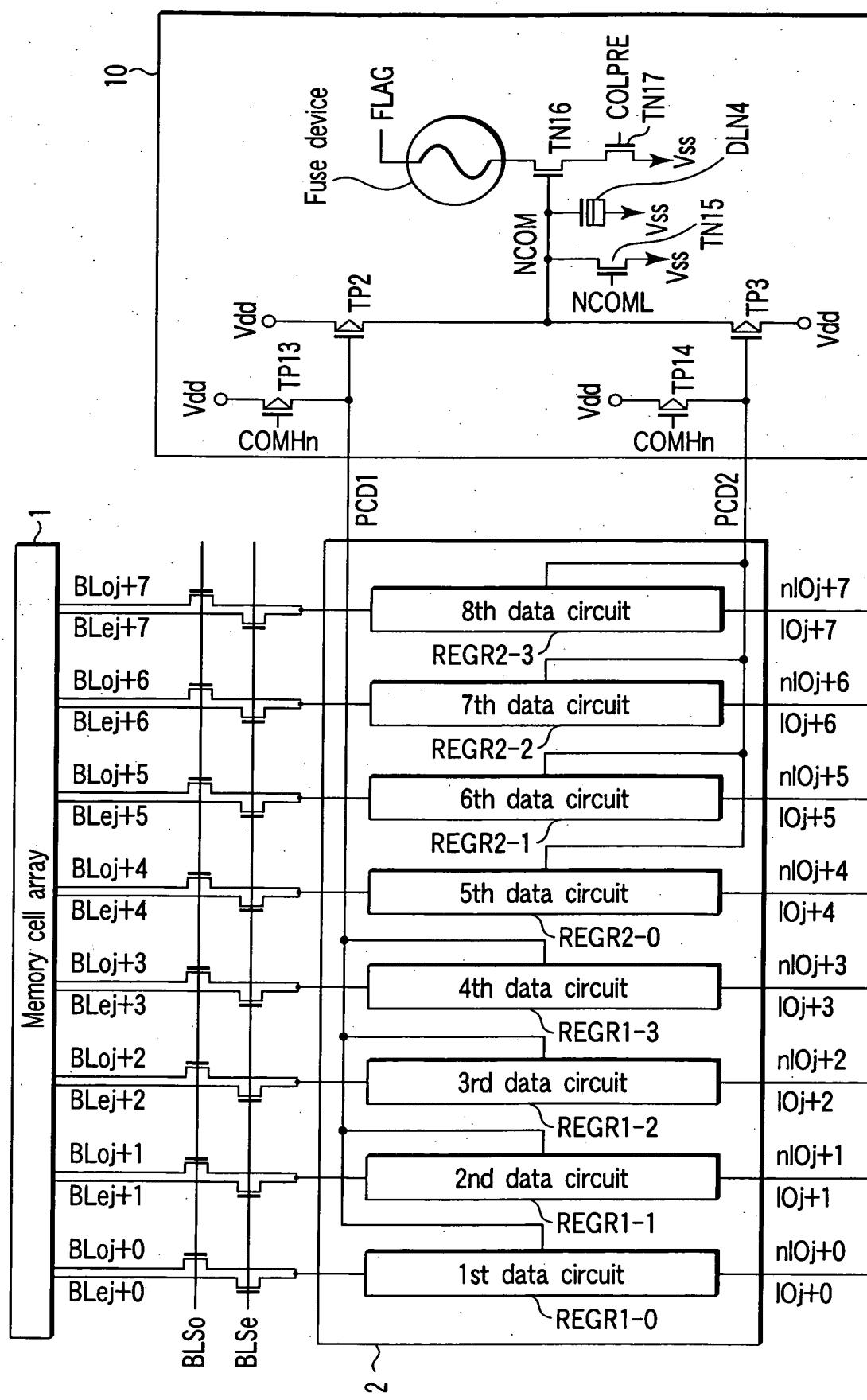


FIG. 8

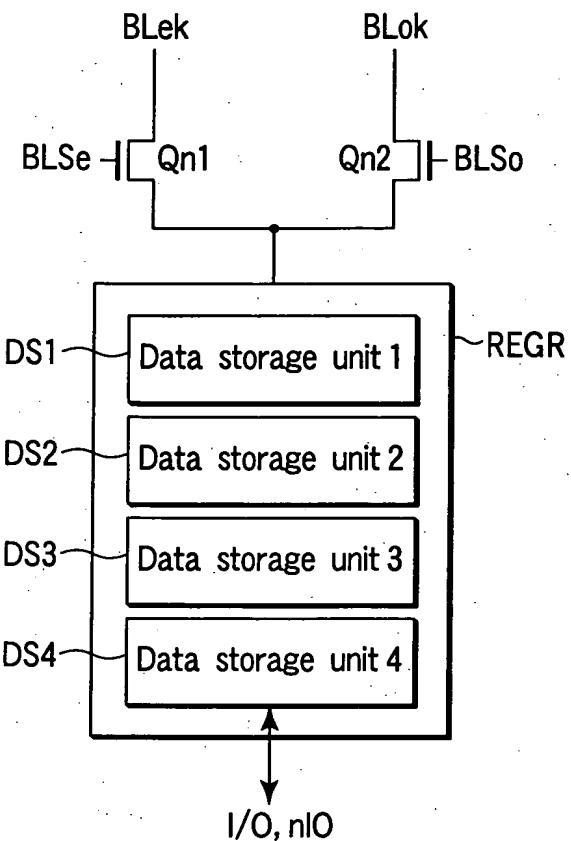


FIG. 9

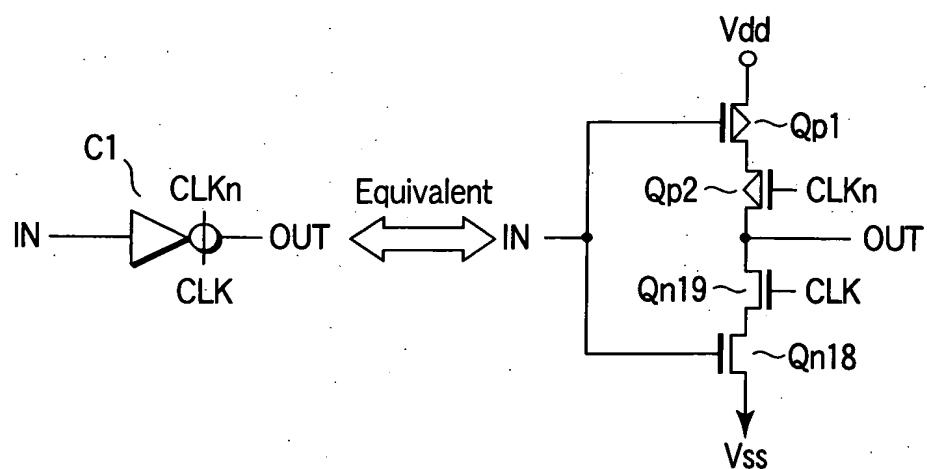


FIG. 11

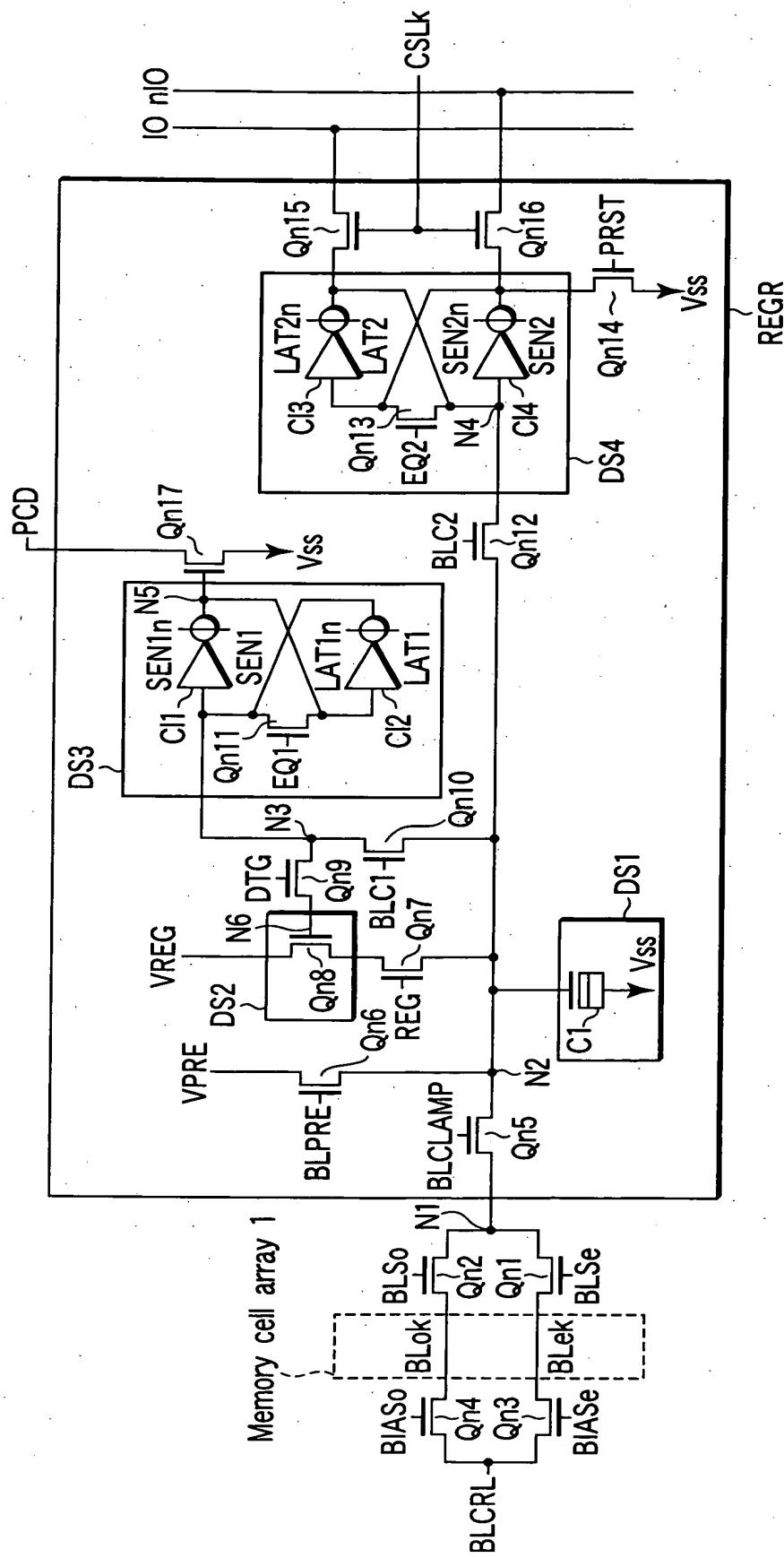
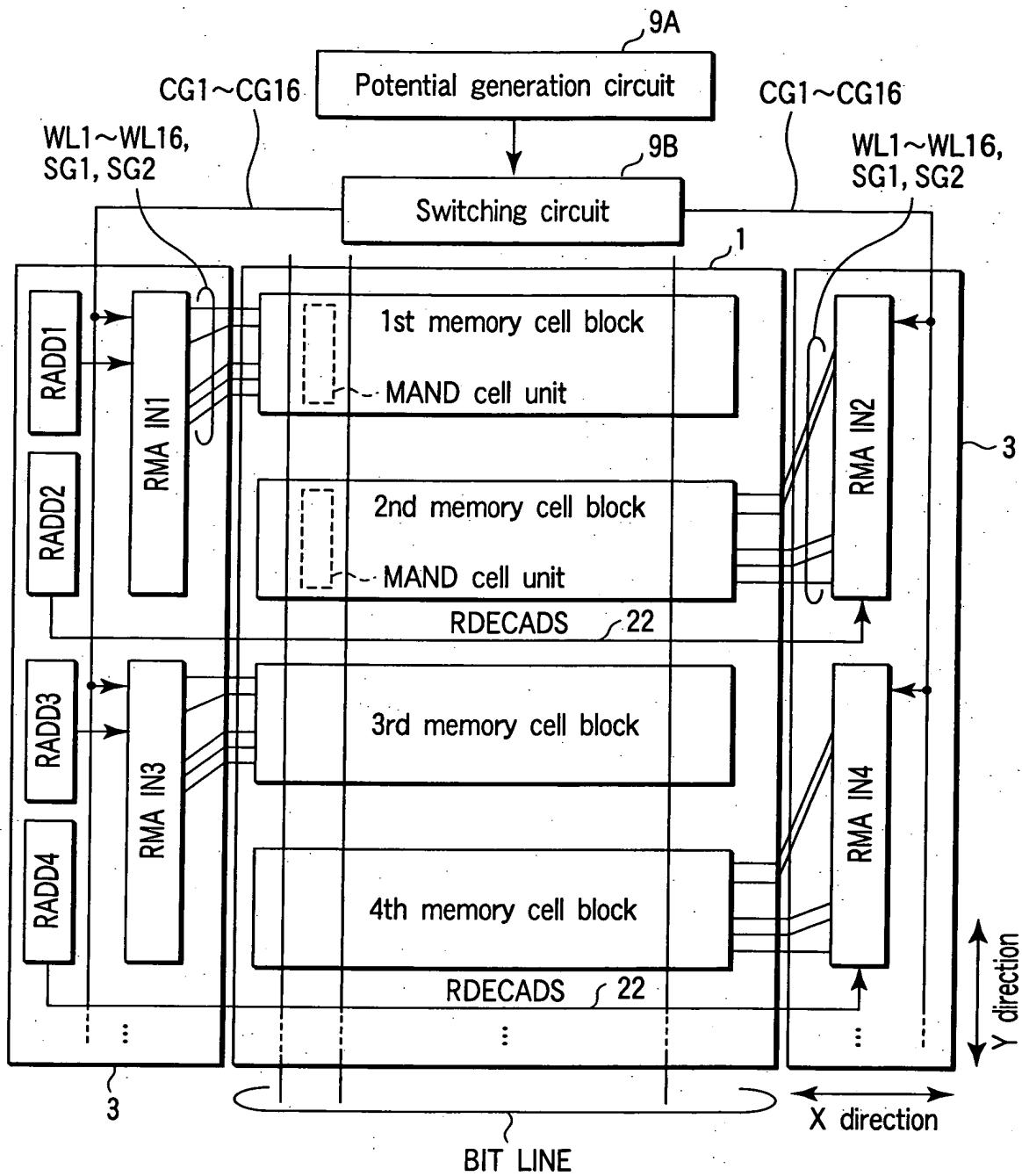


FIG. 10



RMAIN_i : i-th word line driver
 RADD_i : i-th row address decoder
 RDECADS : Word line driver selection signal
 $i=1, 2, 3, 4, \dots$

FIG. 12

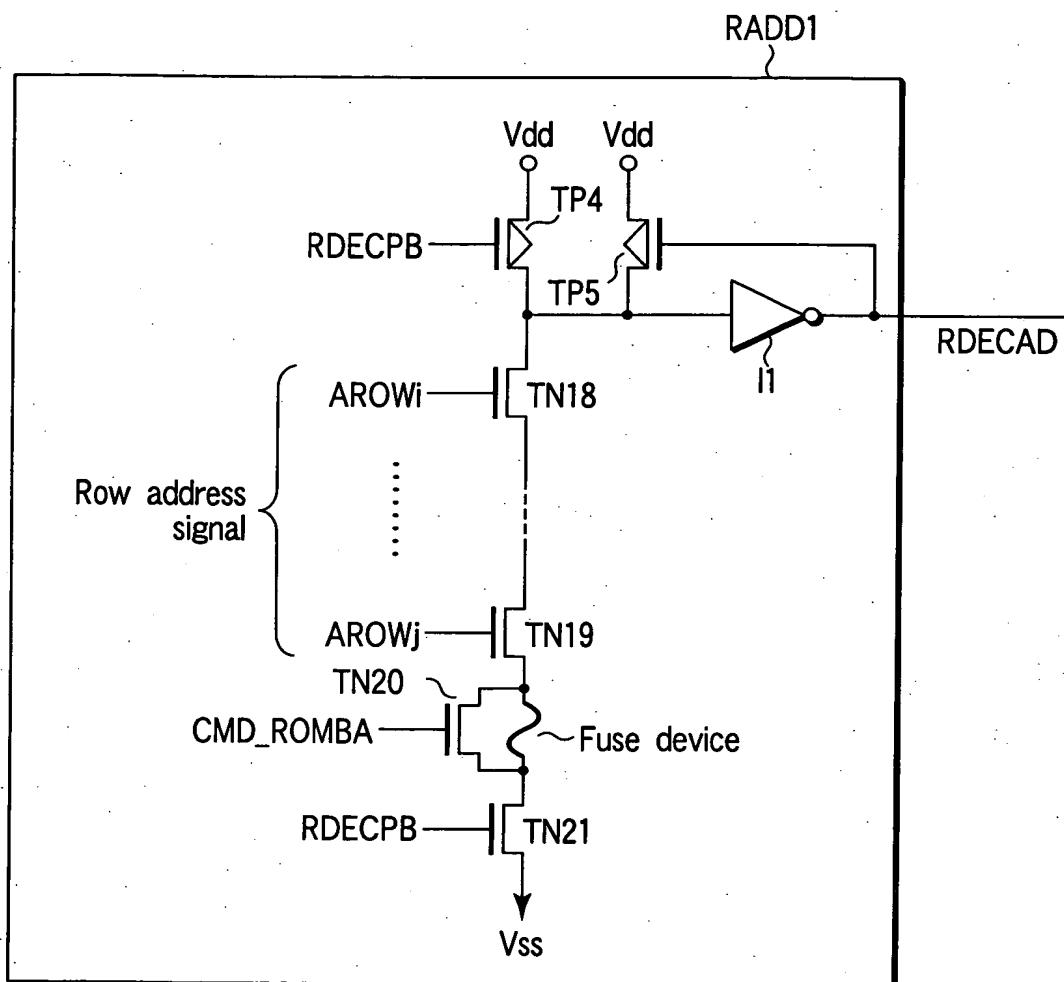
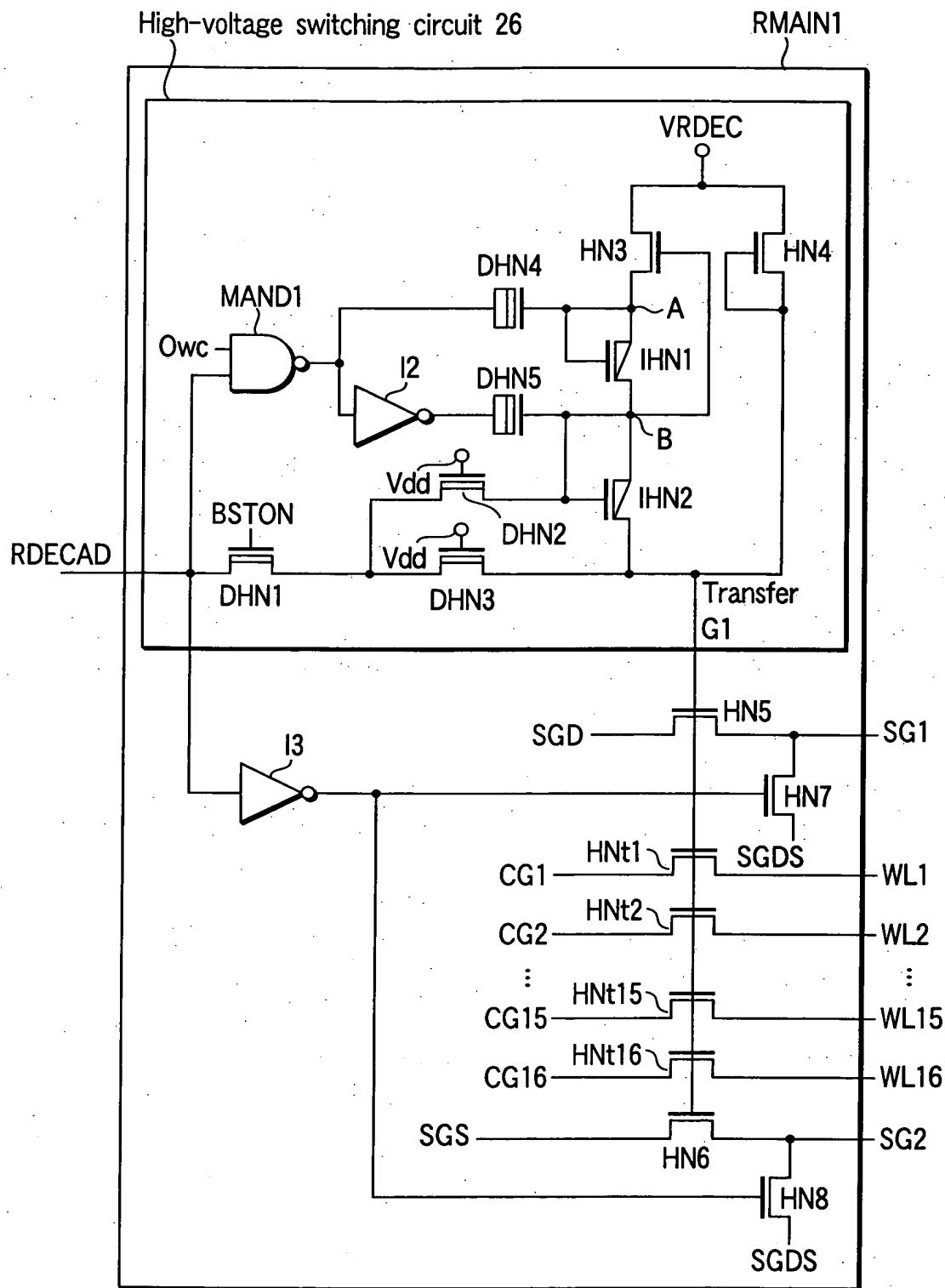


FIG. 13



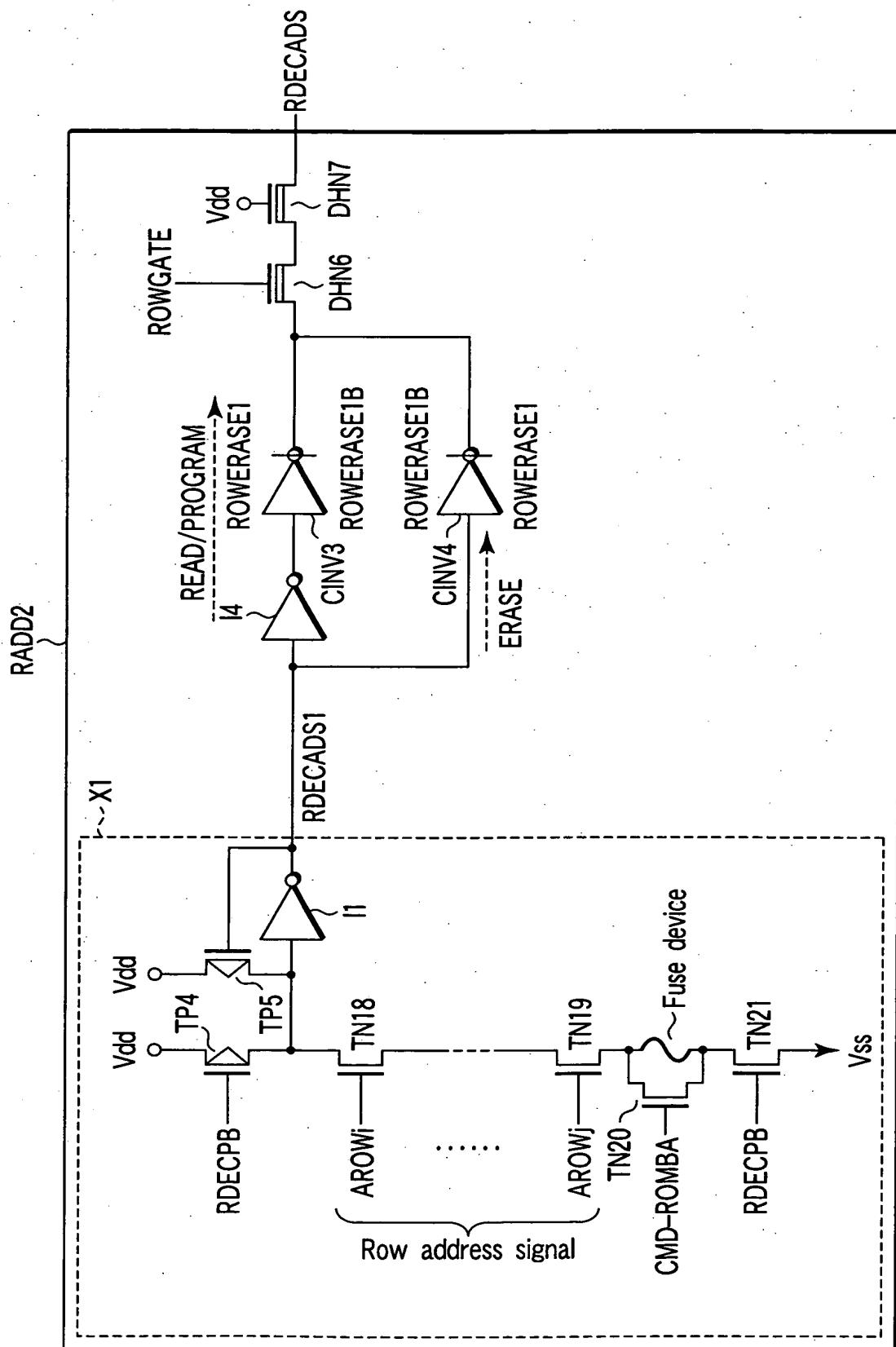


FIG. 15

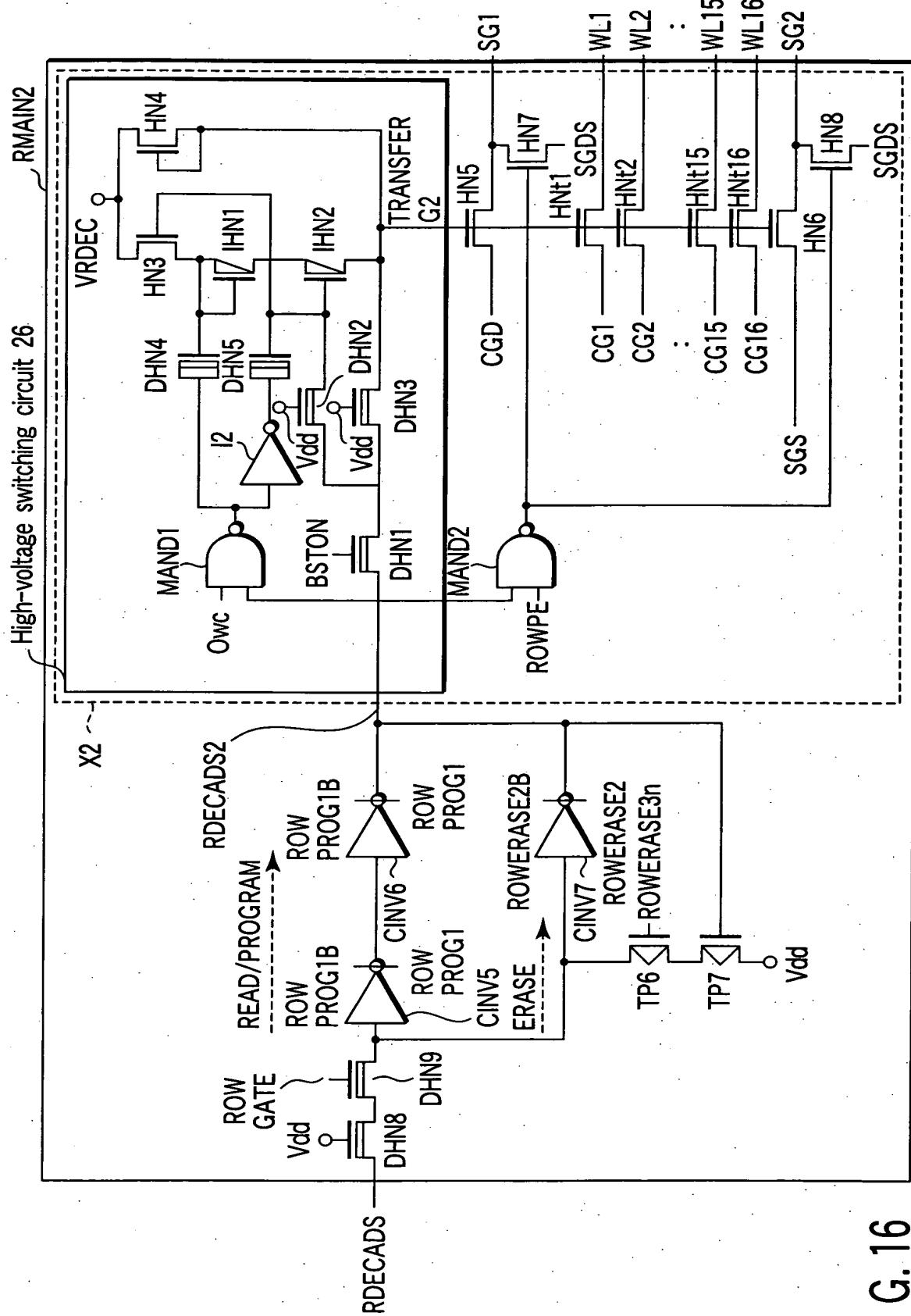


FIG. 16

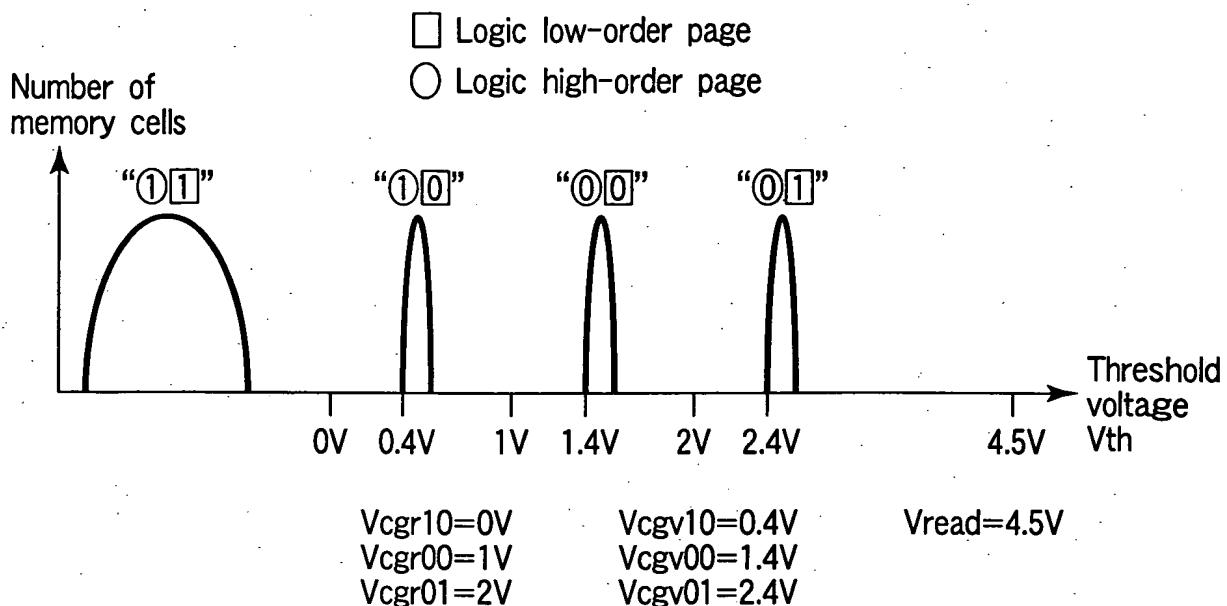


FIG. 17

Program of logic low-order page

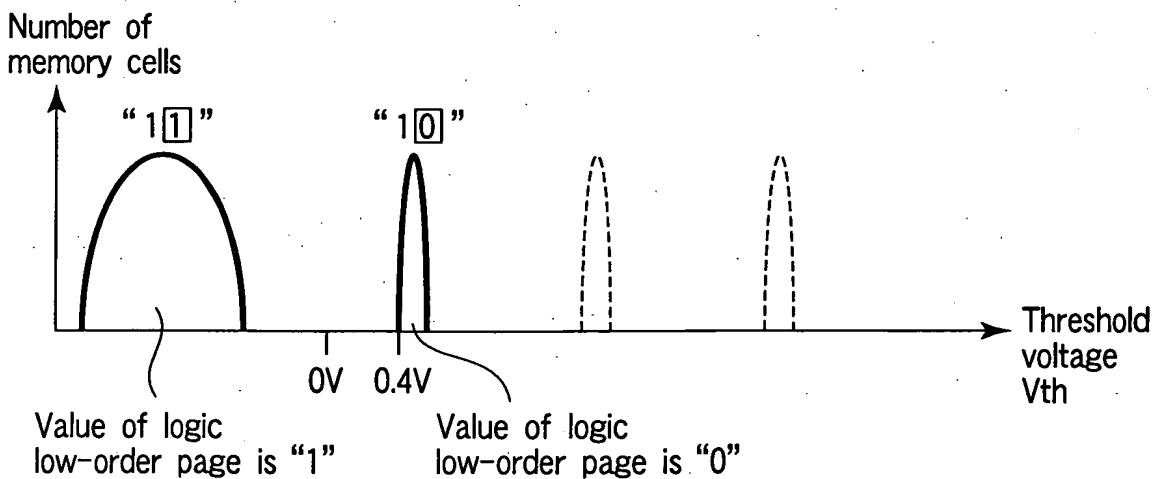


FIG. 18

Program of logic high-order page

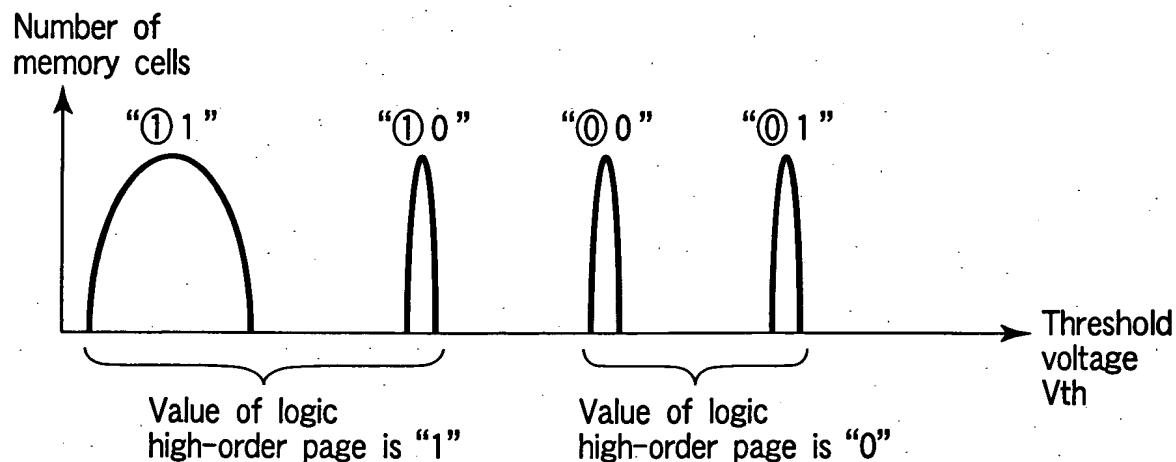


FIG. 19

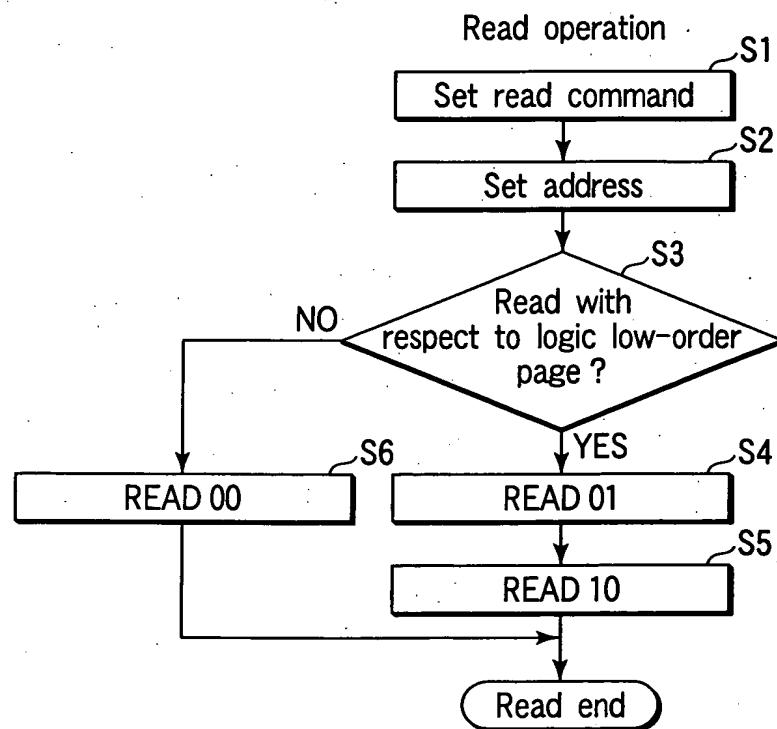


FIG. 20

READ 10/00/01

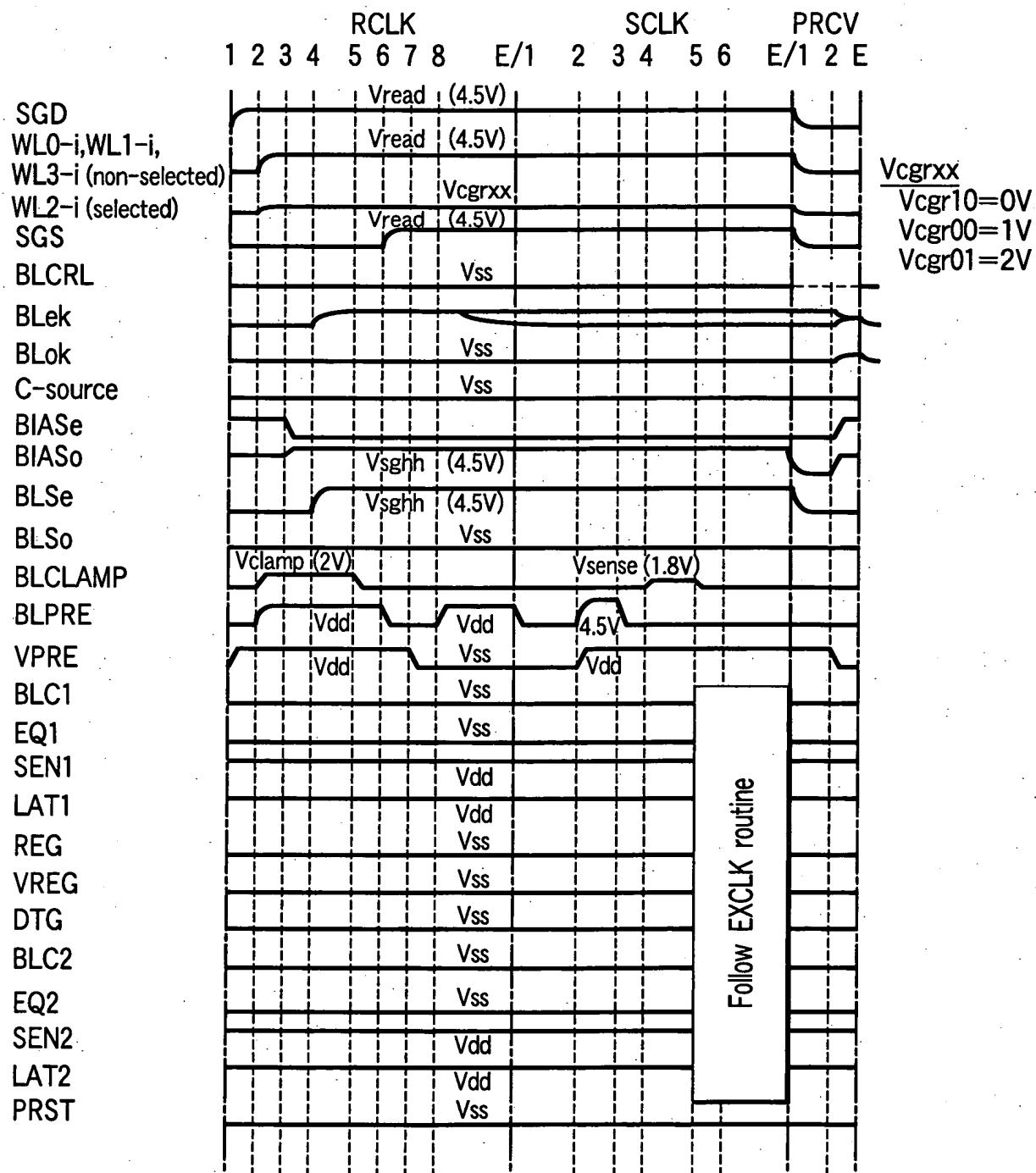
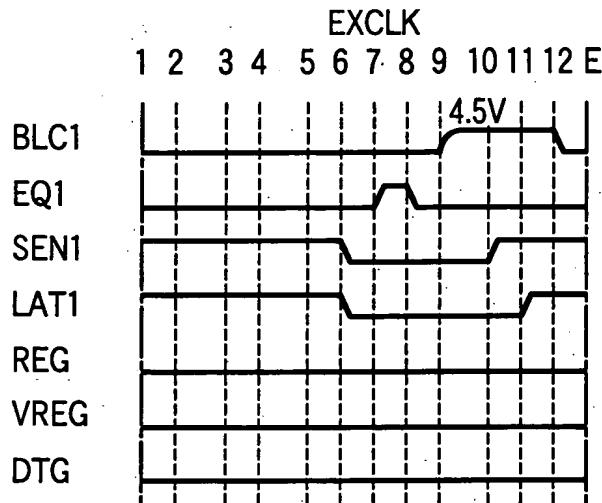


FIG. 21

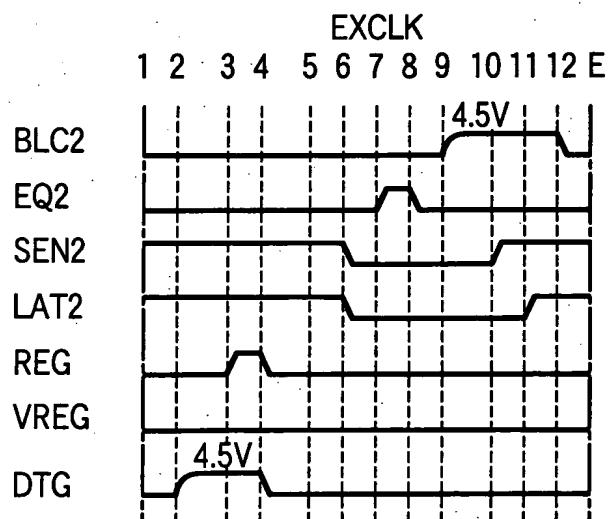
READ01 (EXCLK routine)



No change in signals other than shown signals

FIG. 22

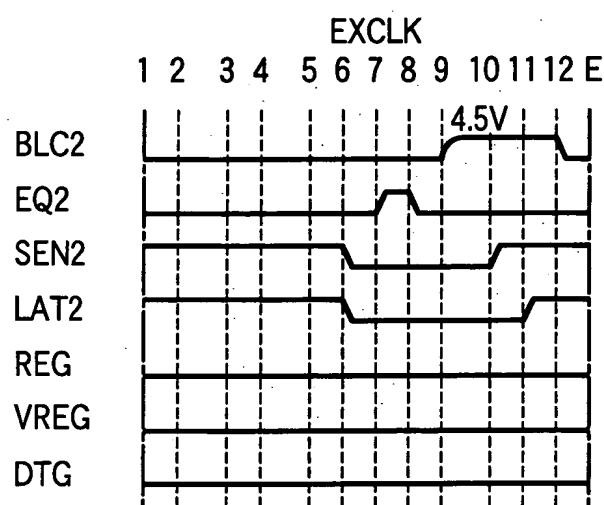
READ10 (EXCLK routine)



No change in signals other than shown signals

FIG. 23

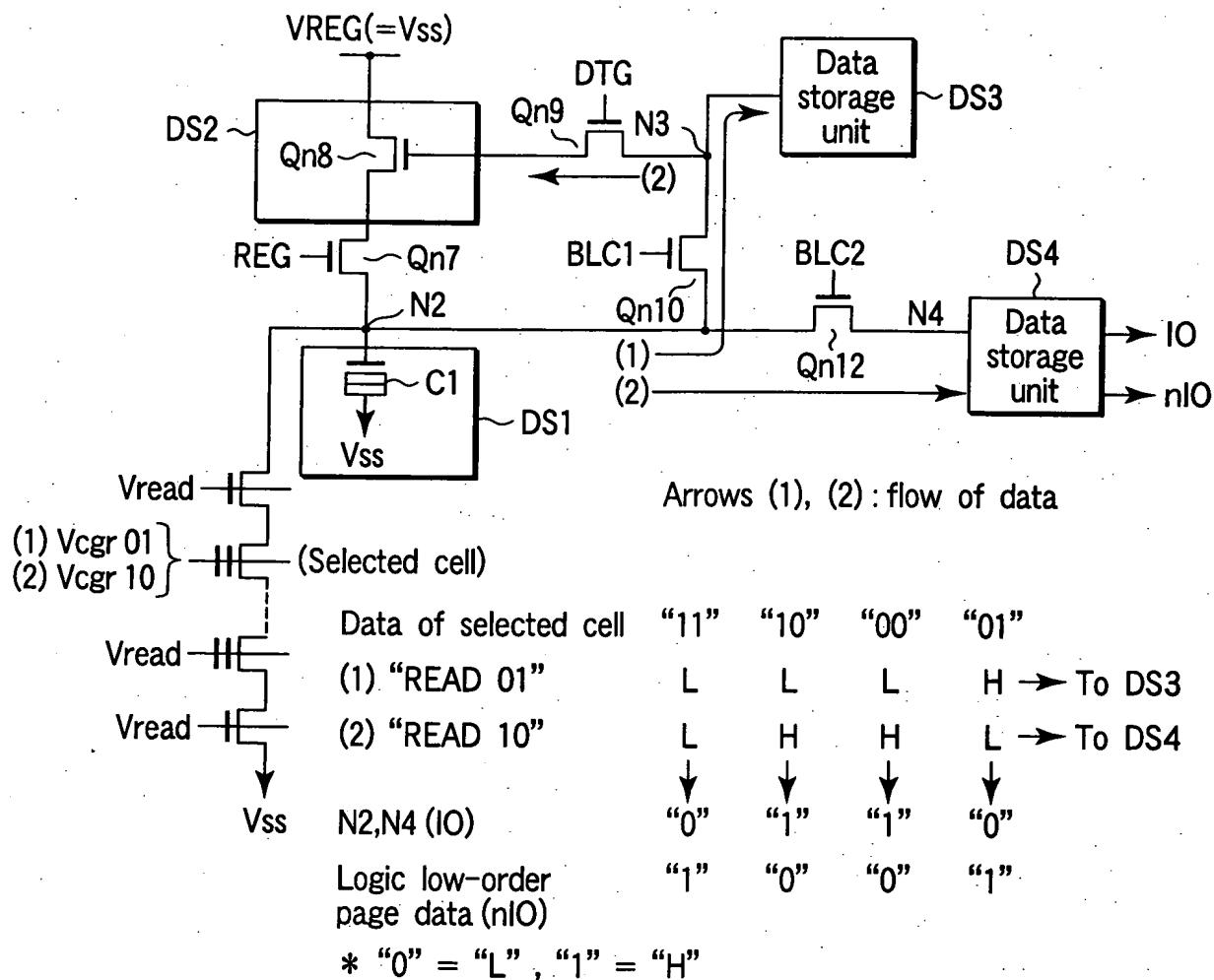
READ00 (EXCLK routine)



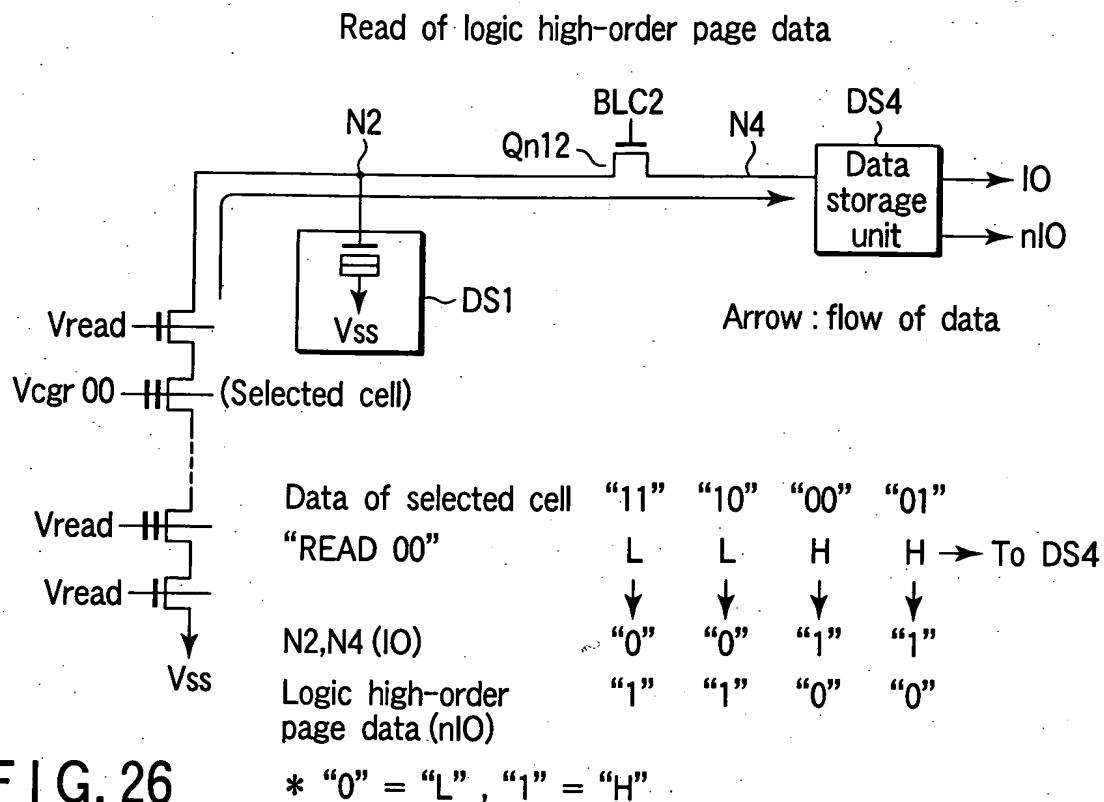
No change in signals other than shown signals

FIG. 24

Read of logic low-order page data



F I G. 25



Program operation 1 (Pass Write)

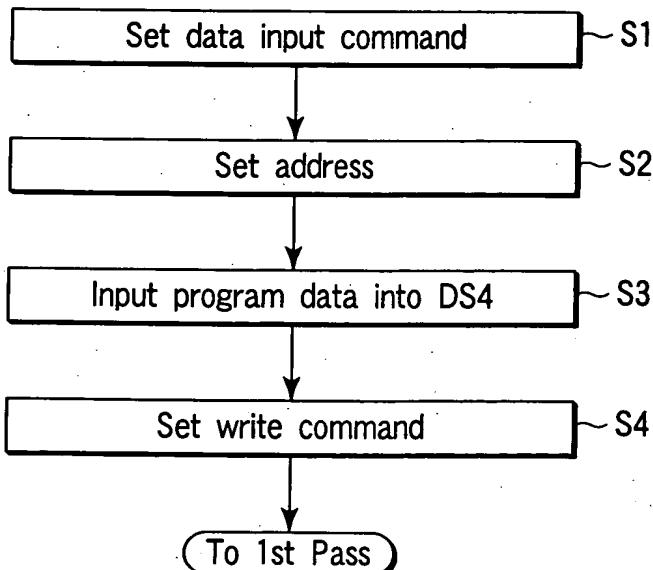


FIG. 27

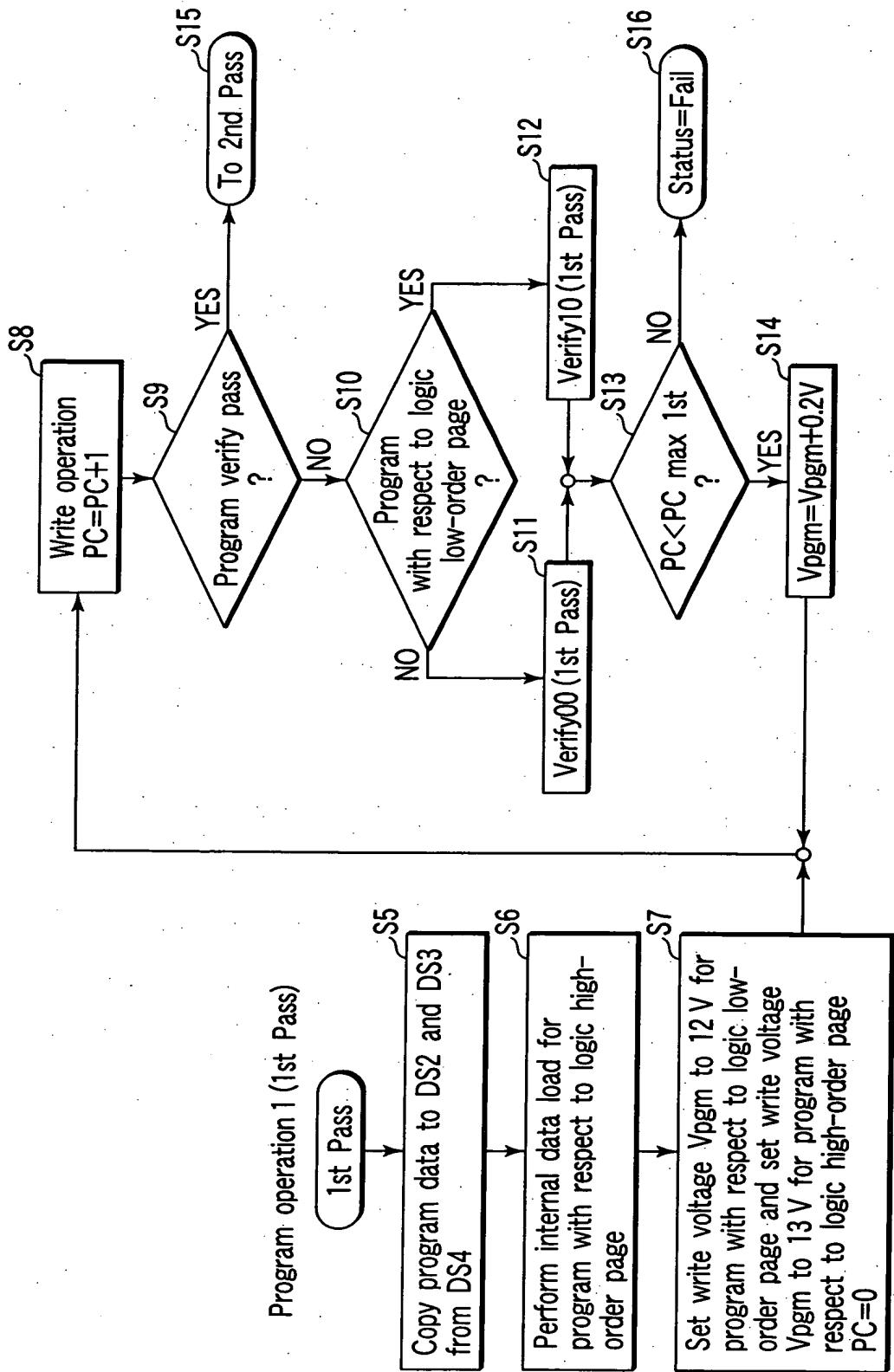


FIG. 28

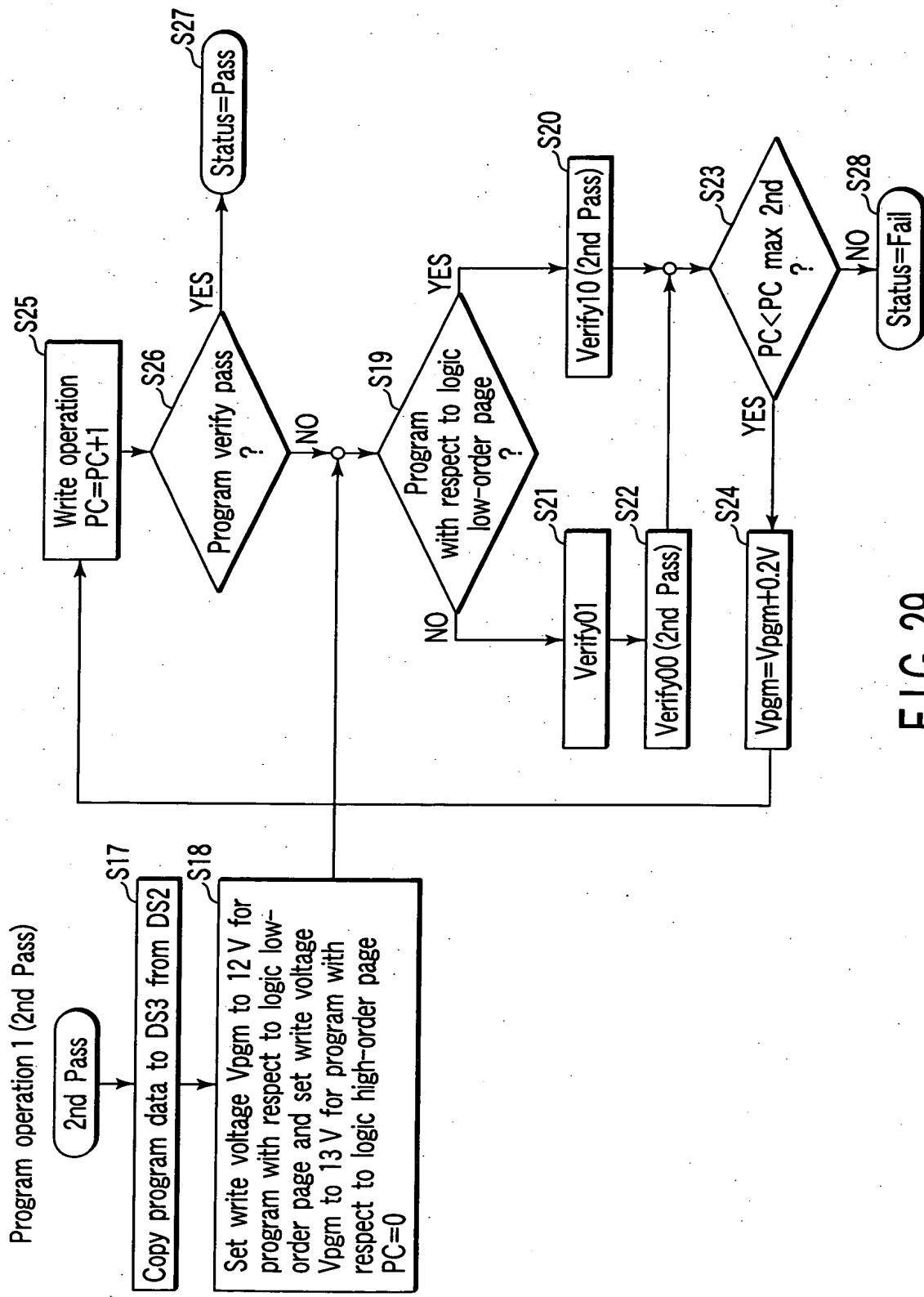


FIG. 29

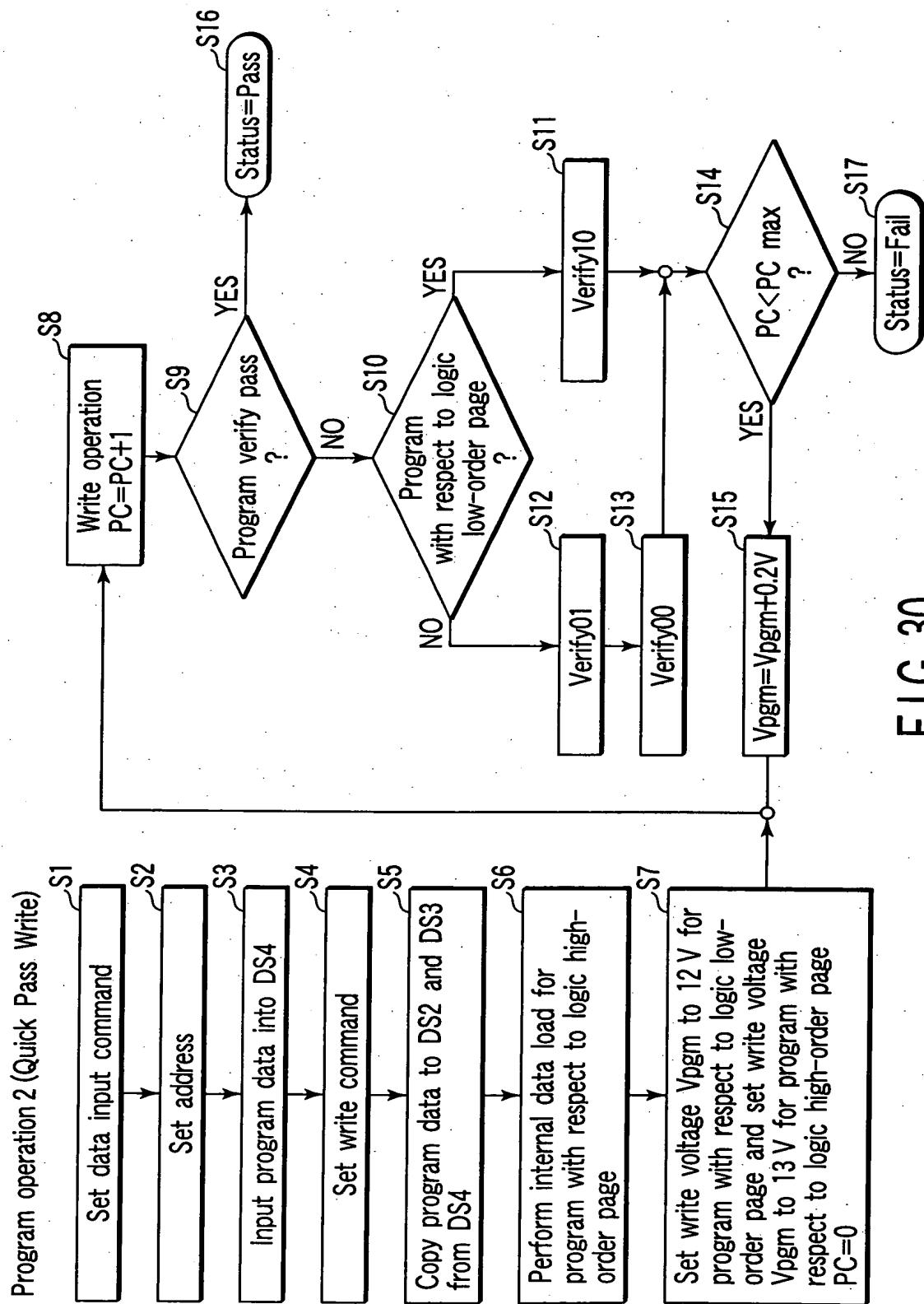


FIG. 30

Copy of program data to DS2 and DS3 from DS4

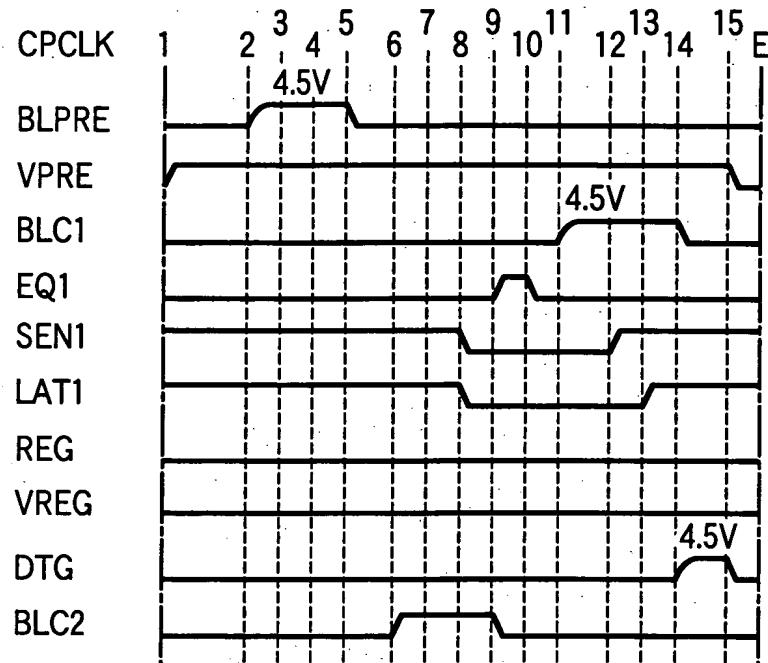
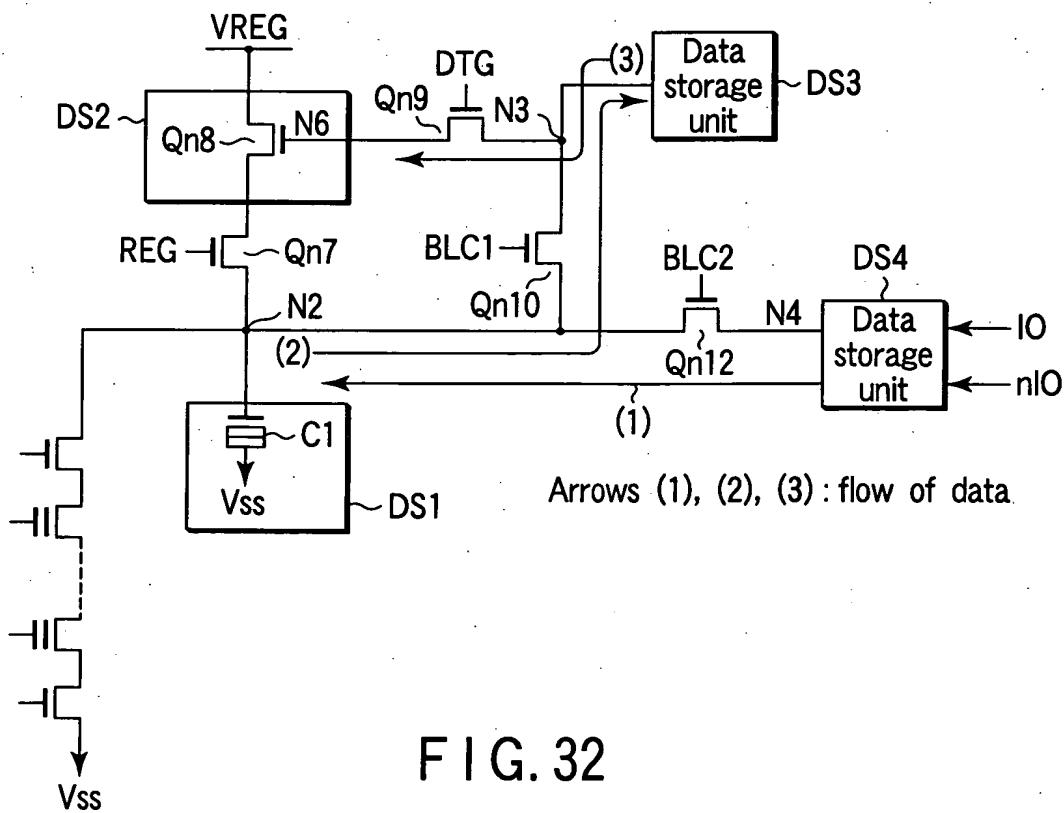


FIG. 31

Copy of program data to DS2 and DS3 from DS4



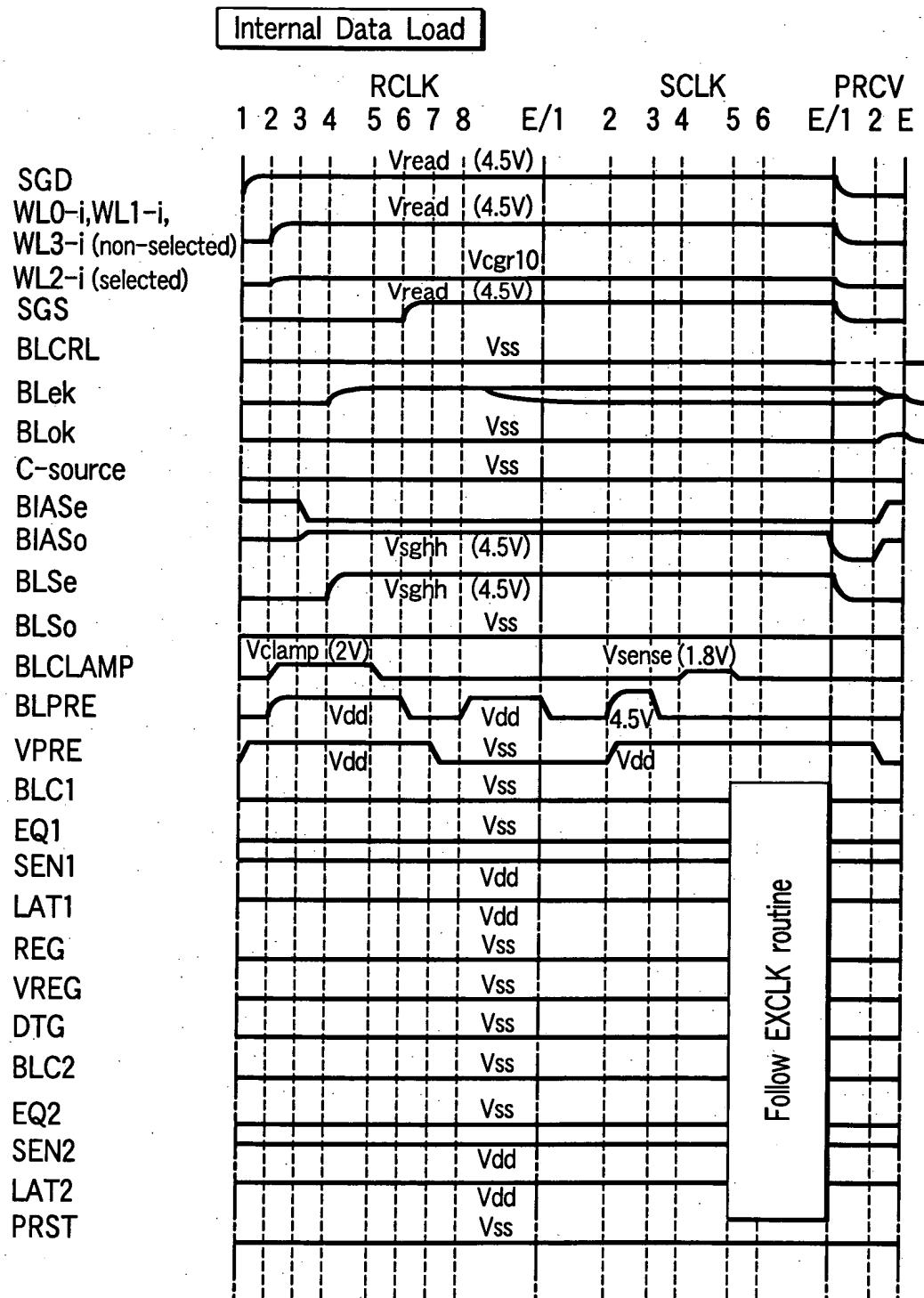


FIG. 33

Internal Data Load (EXCLK routine)

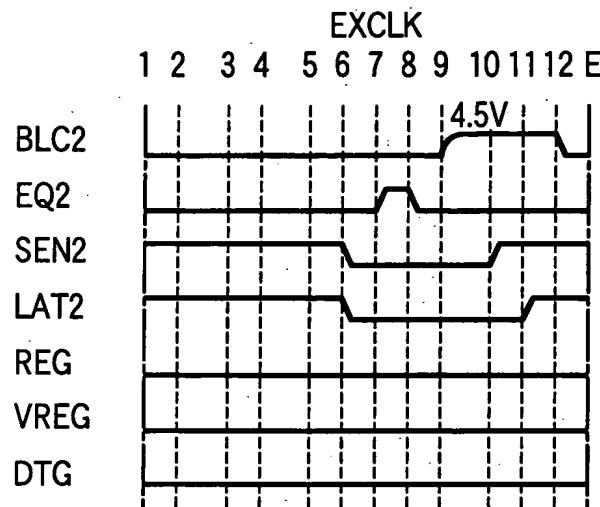


FIG. 34 No change in signals other than shown signals

Internal Data Load

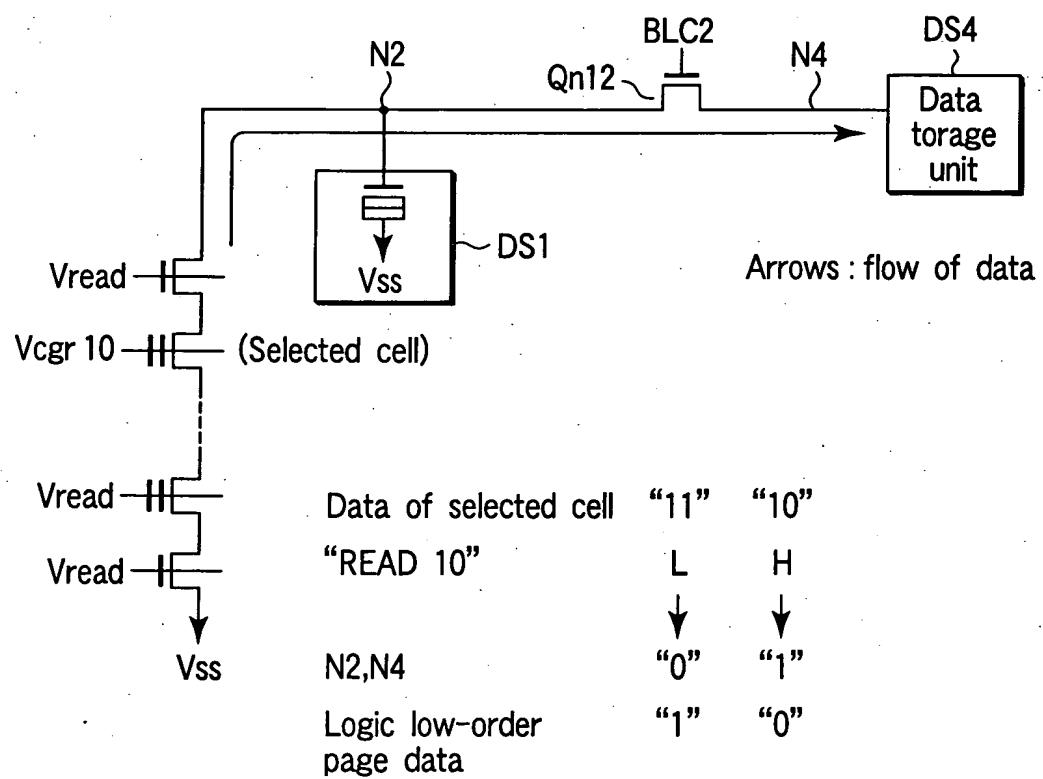


FIG. 35 * "0" = "L" , "1" = "H"

Copy of program data to DS3 from DS2

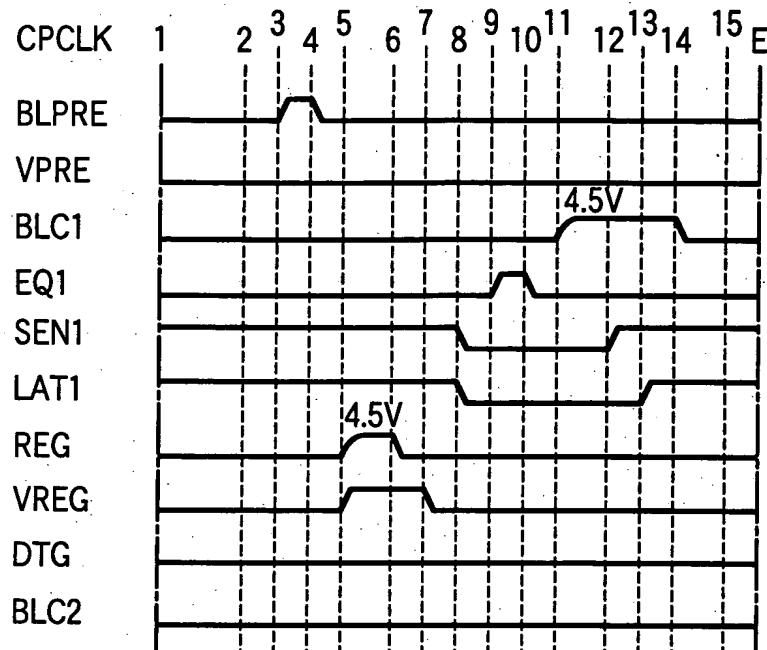


FIG. 36

Copy of program data to DS3 from DS2

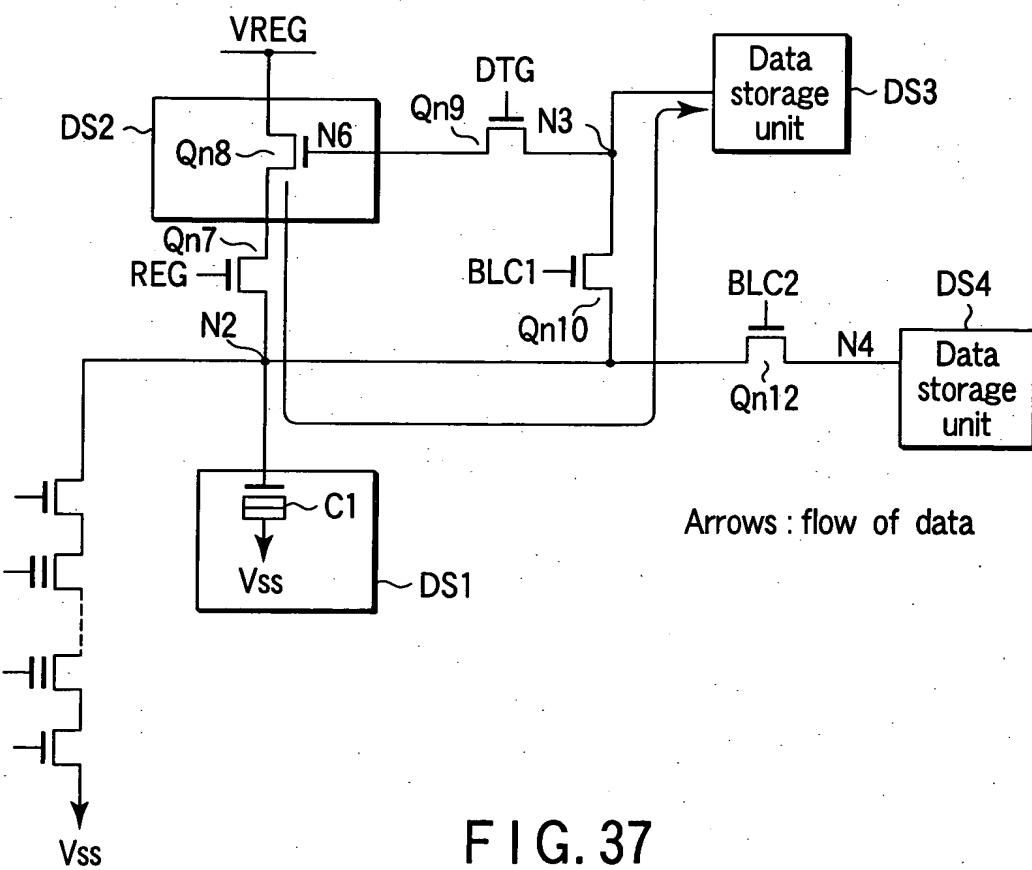


FIG. 37

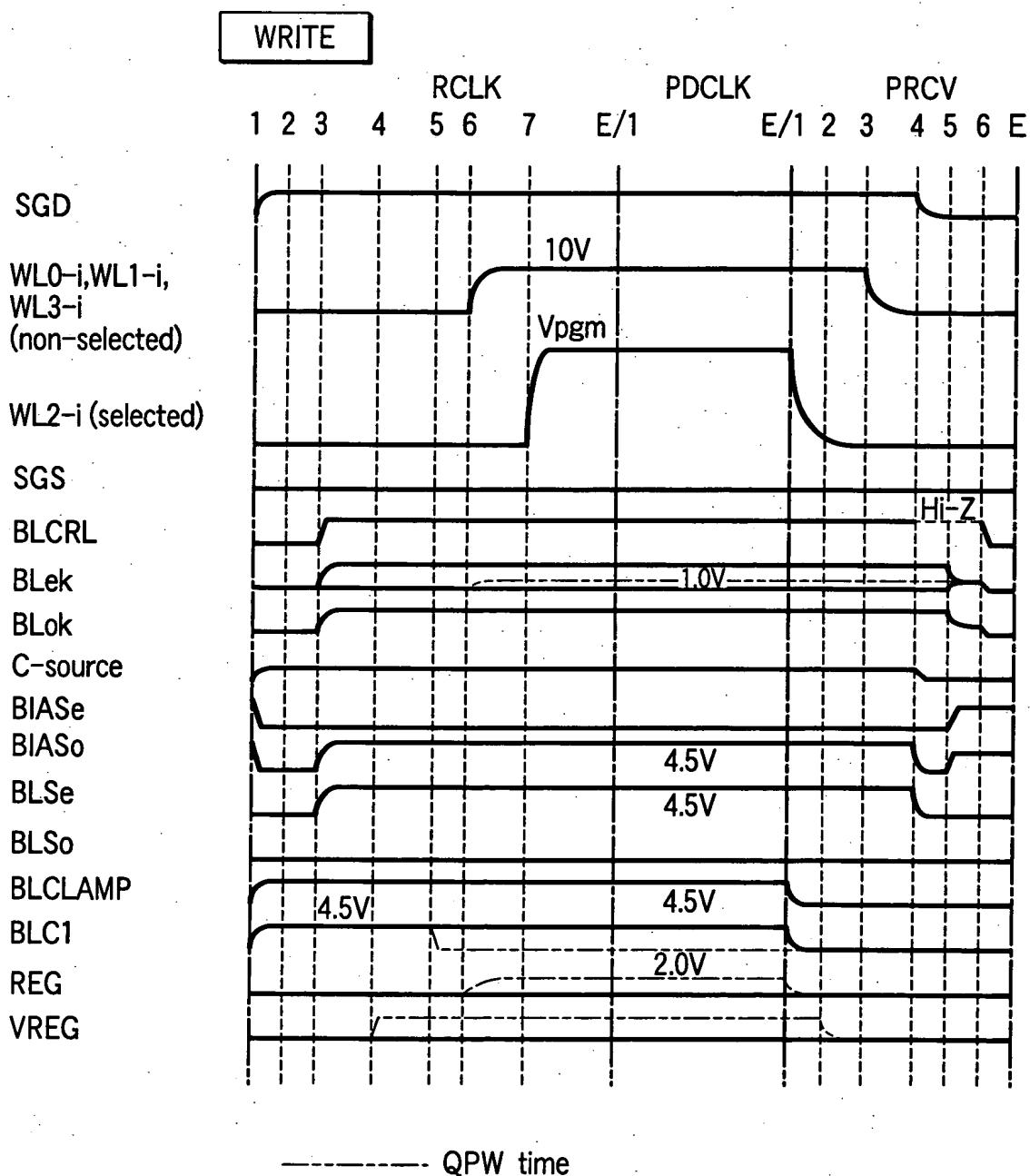


FIG. 38

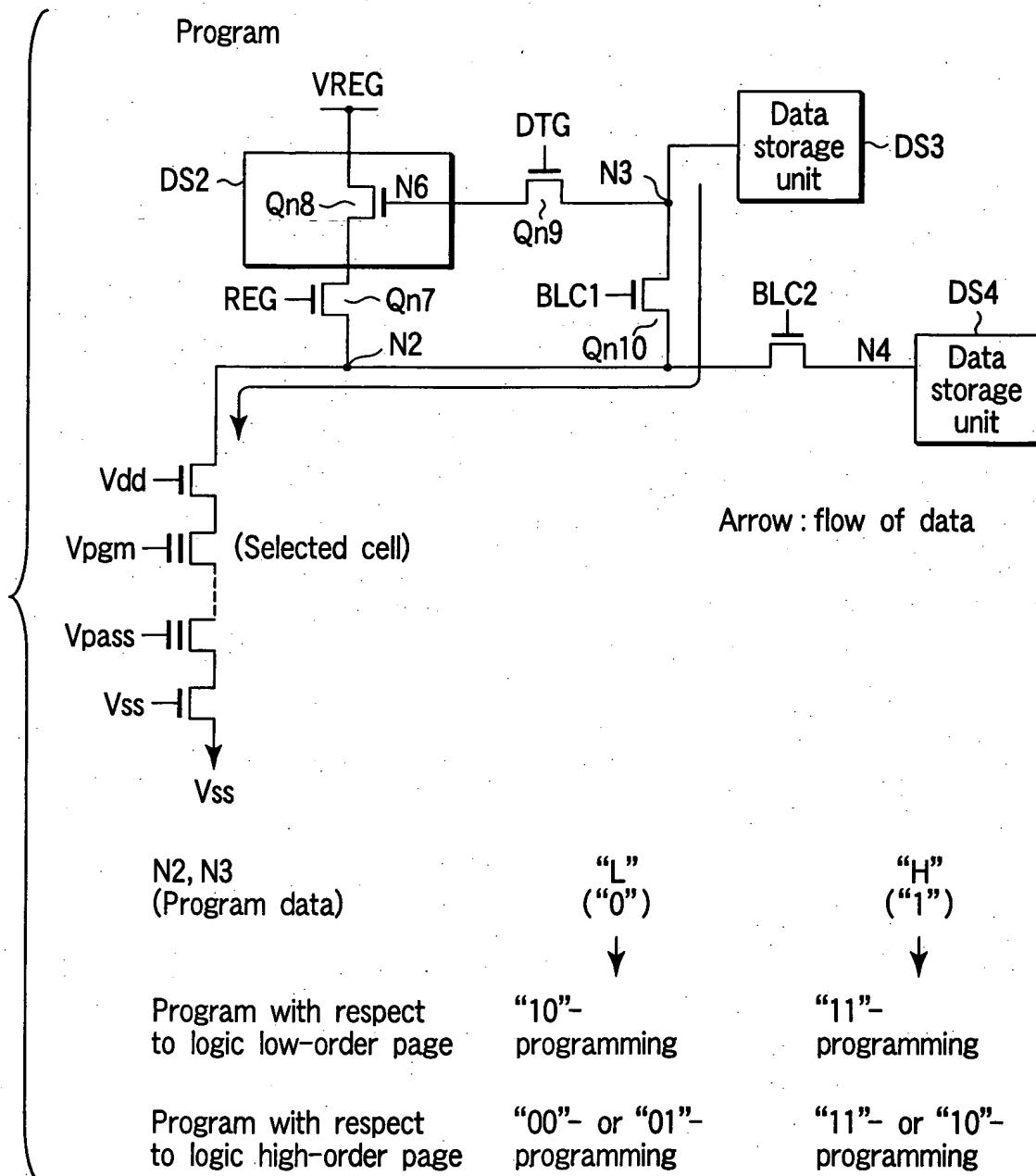
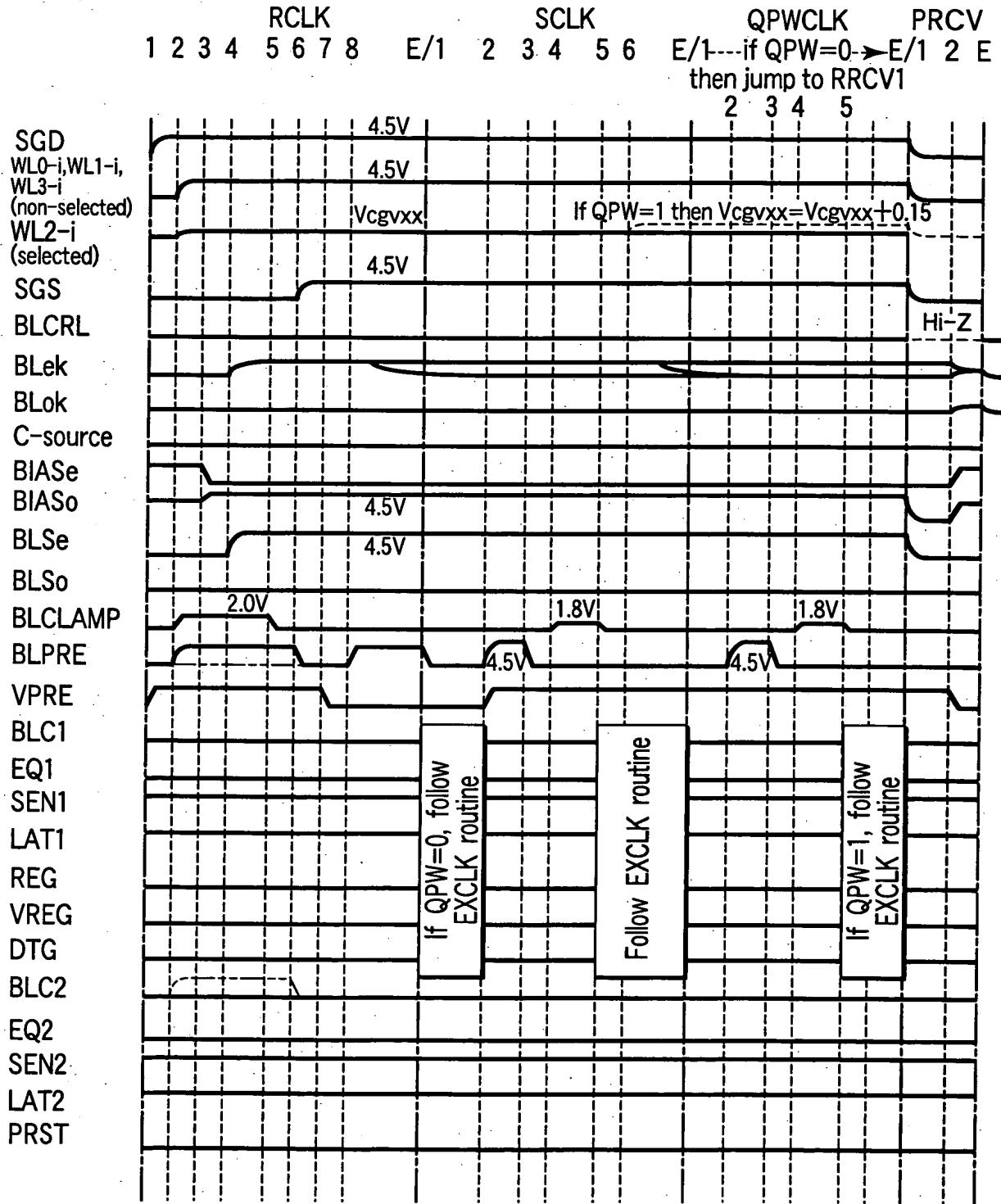


FIG. 39

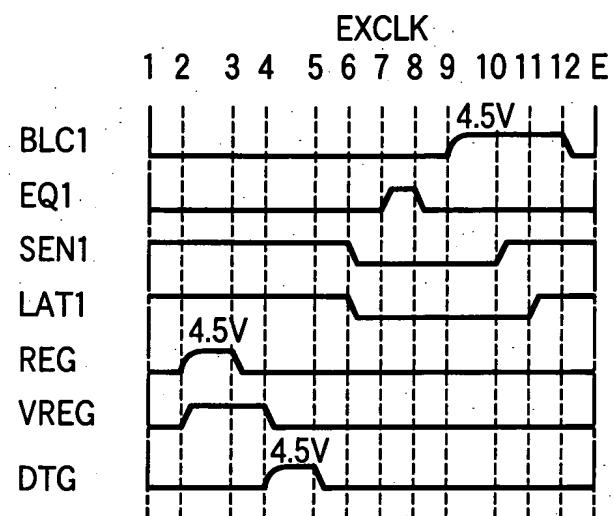
VERIFY 10/00/01



----- Verify00 (2nd Pass) or verify00 at QPW time

FIG. 40

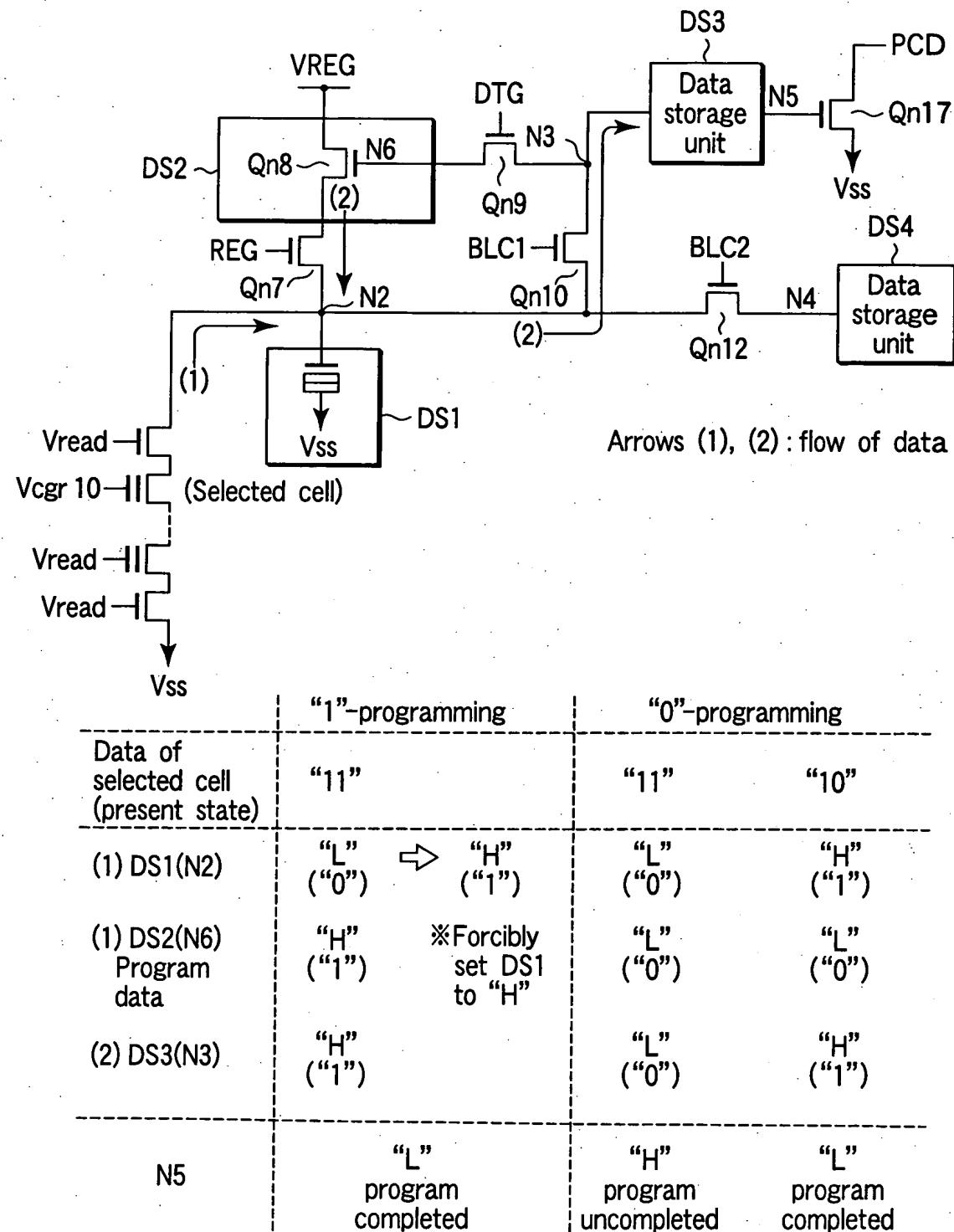
VERIFY10/VERIFY00/VERIFY01
(EXCLK routine)



No change in signals other than shown signals

F I G. 41

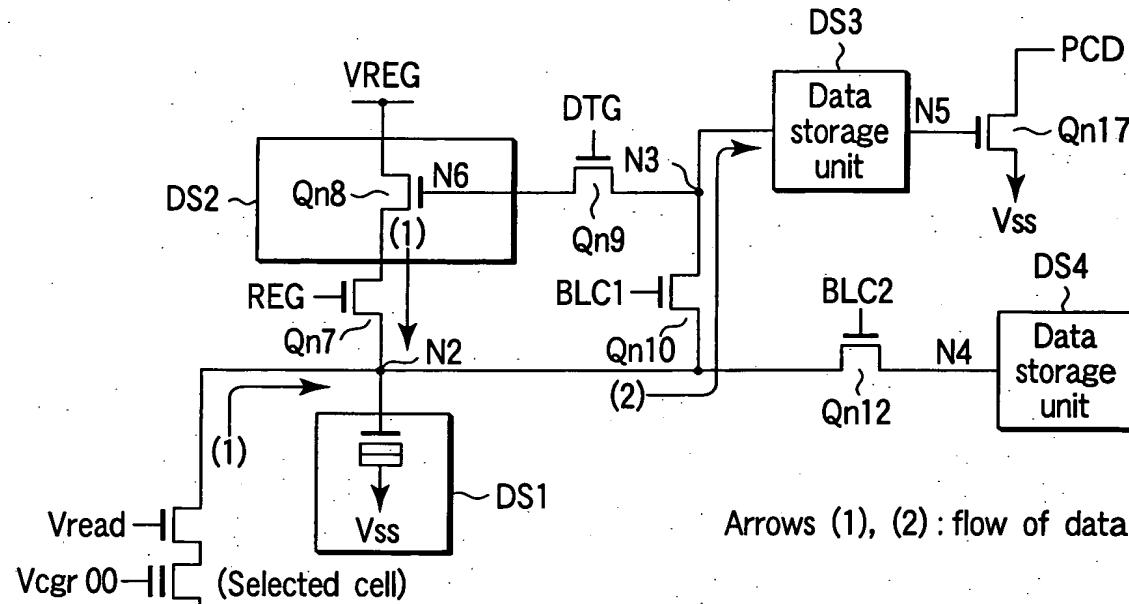
Program with respect to logic low-order page
 "VERIFY 10" + "COMPLETION DETECTION"



※ "Verify 10" includes "verify 10 (1st Pass)" in Write Pass,
 "Verify 10 (2nd Pass)" and "Verify 10" in Qwp

FIG. 42

Program with respect to logic high-order page
"VERIFY 00 (1st Pass)" + "COMPLETION DETECTION"



Vcgr 00 → (Selected cell)

Vread →

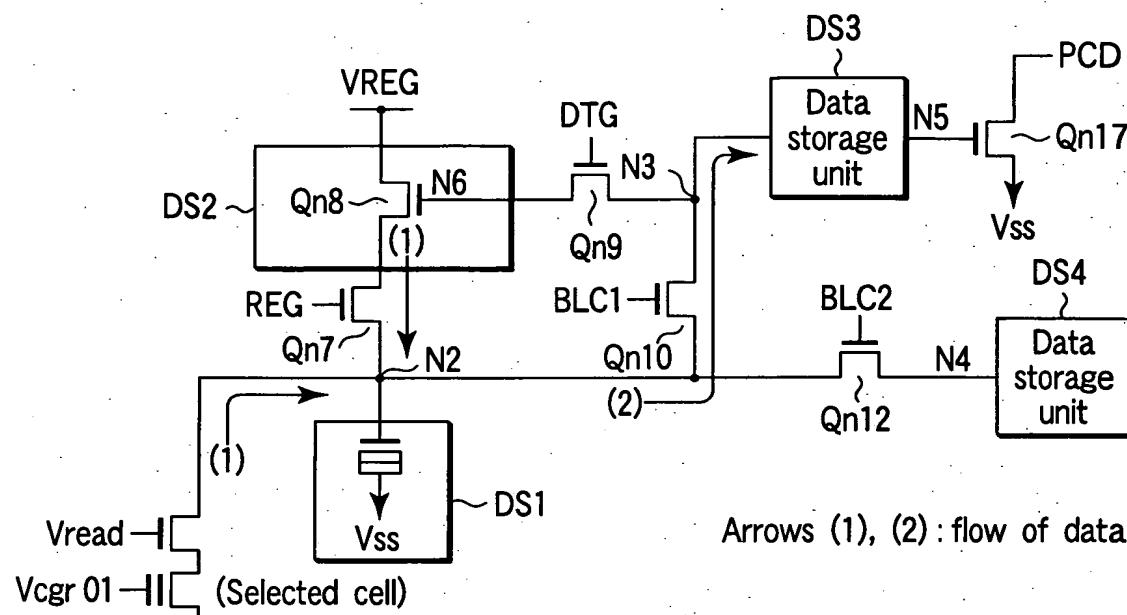
Vread →

Vss

	"1"-programming	"0"-programming
Data of selected cell (present state)	"11" or "10"	"11" or "10" "00"
(1) DS1(N2)	"L" ("0") → "H" ("1")	"L" ("0") "H" ("1")
(1) DS2(N6) Program data	"H" ("1") ※Forcibly set DS1 to "H"	"L" ("0") "L" ("0")
(2) DS3(N3)	"H" ("1")	"L" ("0") "H" ("1")
N5	"L" program completed	"H" program uncompleted
		"L" program completed

F I G. 43

Program with respect to logic high-order page
 "VERIFY 01" + "COMPLETION DETECTION"



	"1"-programming	"0"-programming
Data of selected cell (present state)	"11" or "10"	"11" or "10" or "00" "01"
(1) DS1(N2)	"L" ("0") → "H" ("1")	"L" ("0") "H" ("1")
(1) DS2(N6) Program data	"H" ("1") ※Forcibly set DS1 to "H"	"L" ("0") "L" ("0")
(2) DS3(N3)	"H" ("1")	"L" ("0") "H" ("1")
N5	"L" program completed	"H" program uncompleted
		"L" program completed

FIG. 44

Program with respect to logic high-order page
“VERIFY 00 (2nd Pass)” + “COMPLETION DETECTION”

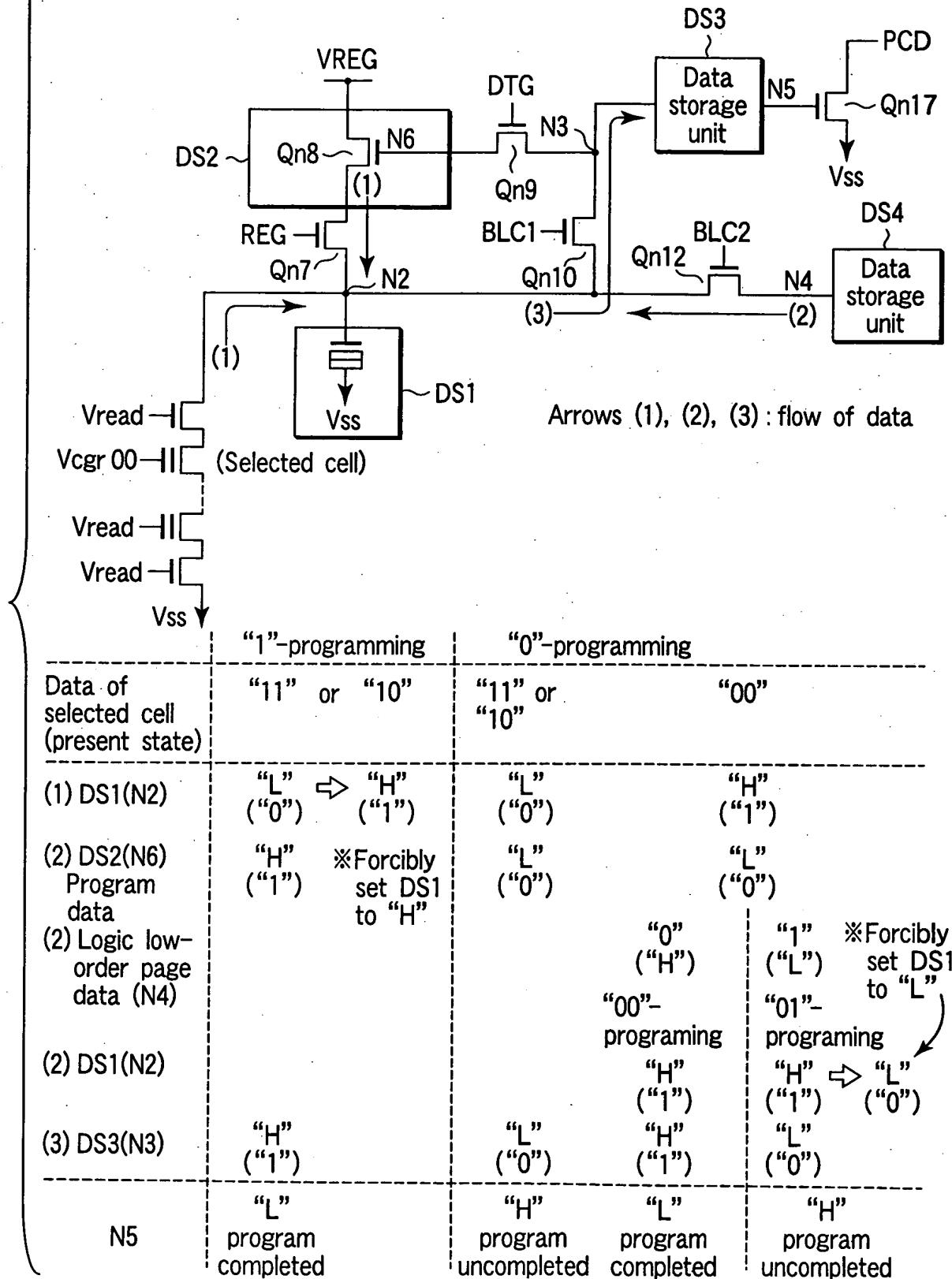


FIG. 45